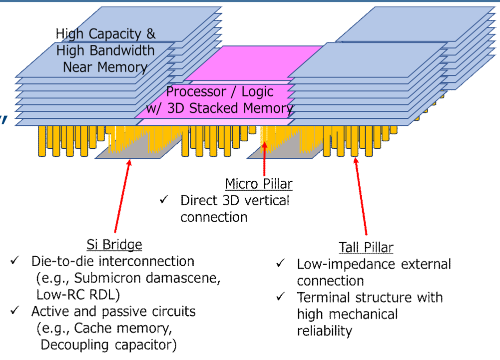
AOI Chiplet Integration Technology

Pillar-Suspended Bridge (PSB)

■ Pillar-Suspended Bridge (PSB) concept

- ✓ Simplified and reliable structure concept
- ✓ A new bridge architecture "Without Interposer"

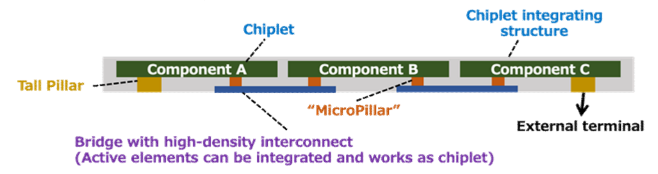


◆Comparison of Integration Technology

(a) Conventional semiconductor integrated circuit (IC chip): Circuits are connected by on-chip wirings.

(b) Conventional Chiplet Integration Structure: Interposer with high-density wiring connects chiplets.

(c) "Pillar-Suspended Bridge (PSB)": Chiplets are connected via bridges without Interposer. (MetaIC: *Integrated Circuit of the Integrated Circuits)*



◆Technical Roadmap

Item	2025	2026	2027	2028	2029	2030	Technical breakthrogh
Die-to-Die I/F Pitch (Development)	40 um Qualify	25 um Prototype	25 um Qualify	15 um Prototype	15 um Qualify	10 um Prototype	Metallization, Bonding Technology
Die-to-Die I/F Pitch (HVM)				40 um		25 um	Automotive / Industry Level Quality
Bridge Min L/S				1/1 um 4 Layers		0.75/0.75 um 8 Layers	Design for Signal Integrity

Automotive Reliability: AEC-Q100 Grade 1 Level

◆Specifications of the model and TEG chips

Item	Value
Module Size	10.60 mm X 14.94 mm
Chiplet-TEG 1 and 2 Die Size	10.00 mm X 7.00 mm X 0.70 mm
Bridge-TEG Die Size	10.00 mm X 1.00 mm X 0.11 mm
Number of Pads on Chiplet-TEG	2240
Number of Pads on Bridge-TEG	2250
MicroPillar Pitch	40 μm
MicroPillar Diameter	25 μm
MicroPillar Thickness	10 μm
Tall Pillar Pitch	142 μm
Tall Pillar Diameter	70 μm
Tall Pillar Thickness	120 μm
Thickness of 1st Mold	700 μm
Thickness of 2nd Mold	120 μm
Total Module Thickness	820 μm

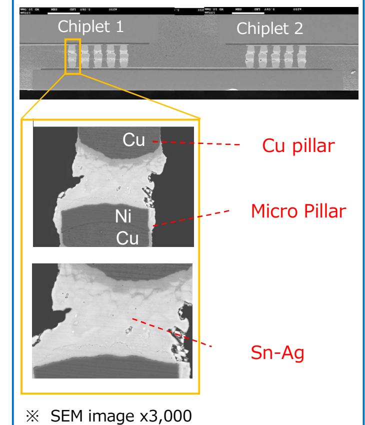
◆Reliability test conditions

Item	Condition
HTS	150° C
TCT	-65° C (15 min) ⇔ RT (2 min) ⇔ 150° C (15 min)
THS	80° C, 85%RH
PCT	121° C, 100%RH, 2 atm

◆Reliability test results

Test	n					
HTS	n=22	100hr	300hr	500hr	1000hr	2000hr
		0/22	0/22	0/22	0/22	0/22
TCT	n=21	100cy	300cy	500cy	1000cy	-
		0/21	0/21	0/21	0/21	-
THS	n=22	100hr	300hr	500hr	1000hr	-
		0/22	0/22	0/22	0/22	-
PCT	n=21	100hr	200hr	-	-	-
		0/21	0/21	-	-	-

● Die-to-Die Interconnection after 2,000h HTS in Passed sample



※ SEM image x3,000

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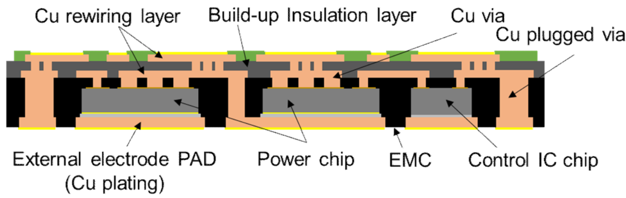
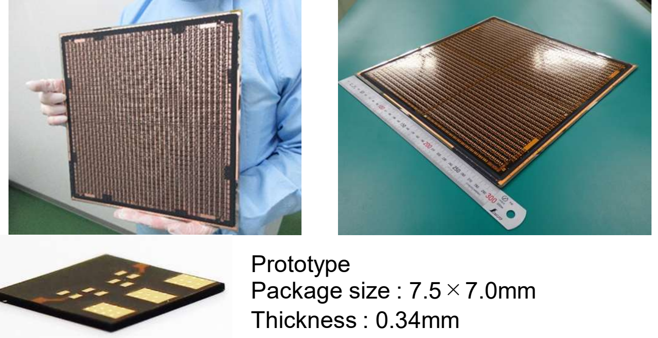
Advanced Power Panel-level Package Technology

DC-DC half-bridge application (GaN HEMT module)

Focusing on power application using chip-embedded technology

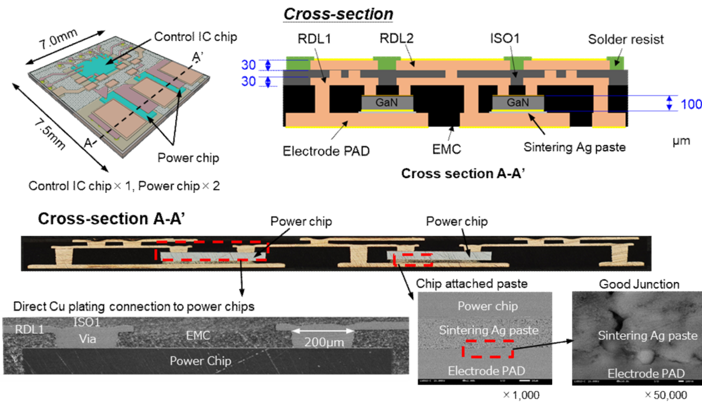
- 300 mm square Panel Form
- Miniaturization and Thinner
- Higher current density
- Excellent double-sided cooling concept
- Robust all Cu plated interconnects



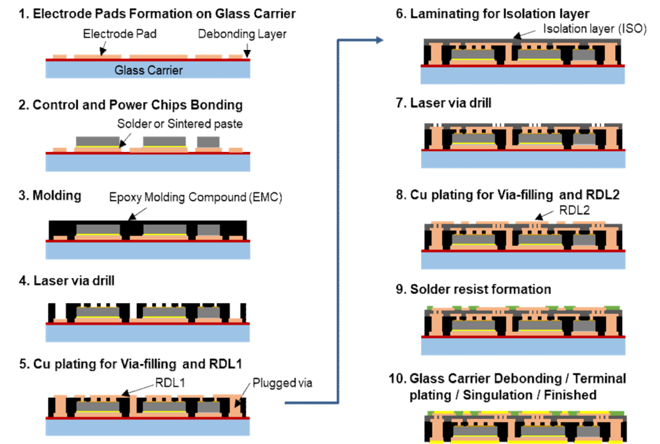


Prototype
Package size : 7.5×7.0mm
Thickness : 0.34mm

Trial production and evaluations for a Prototype



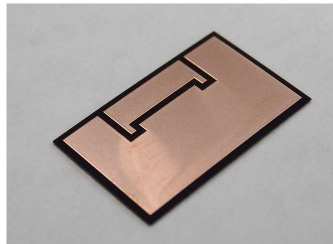
Process flow *From panel substrates to package assembly in-house*



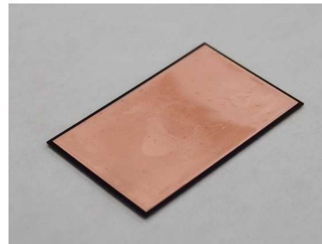
Inverter application (SiC Sub assembly module)

Prototype

Top

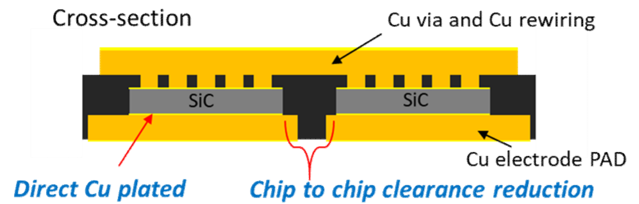


Bottom

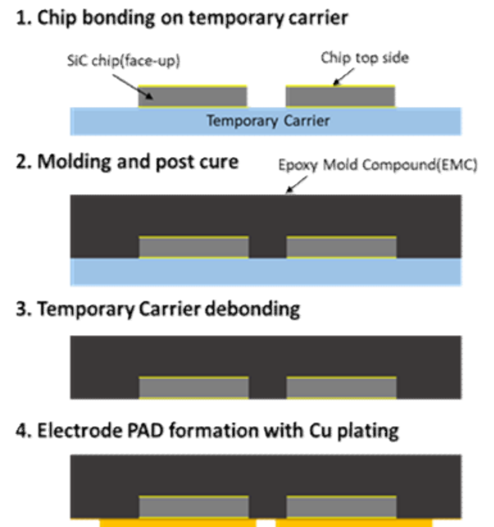


Module size : 15×10mm SiC chip : 2 parallel

Direct double-sided Cu plating connection to SiC chip



Process flow



■TCT results for Direct Cu plated

Reliability test conditions（Component Level Reliability）

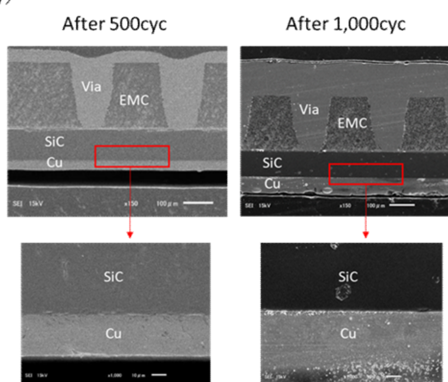
Test Items	Condition
Pre-Condition	The baking condition is 125 ℃ 24h. MSL = LEVEL1 Ta=85℃, RH=85%, storage=168h Reflow soldering heat stress (3times)
Thermal Cycle Test (TCT)	Ta= -65℃⇔150℃

Reliability test results

		Time	100 cycles	300 cycles	500 cycles	1,000 cycles
TCT	n=22	Result (Failure rate)	0/3	0/3	0/3	0/3

※Result :Cross-sectional SEM check by sampling

Cross-sectional SEM after each cycle



No delamination and cracking

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