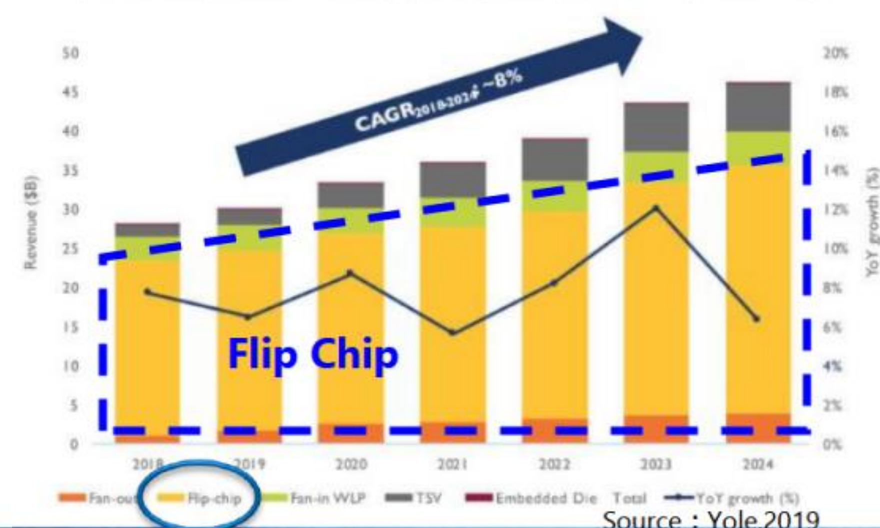
Flip Chip QFN with Cu-pillar

Market Trends

(Source:Yole Développement)



Source：Yole,2019

Source：Yole,2015

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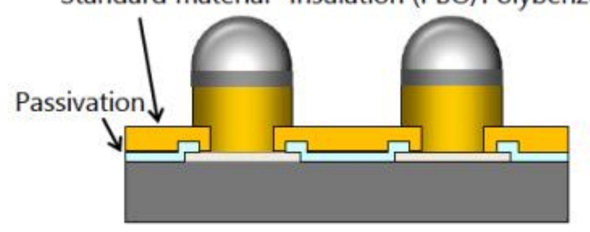
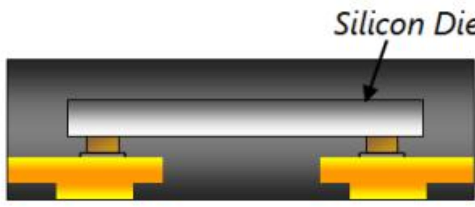
Flip Chip QFN with Cu-pillar

◆ **OUME Electronics ：Cu Pillar Bump**
Over 10 years of experience



- Form solder height up to ½ of pillar dia.
- Formable up to 20um Pillar dia.
- RDL lamination layer
  (Sample result; 3 layers)
  ...Under development



- Flip-chip C4.
- Large format matrix Lead flame
- Wettable flank
  ...Under development

①Sub 6GHz(RF) ：RF-Switch/Antenna Tuning Switch etc.
⇒Low Coff, Low Insertion loss

②Power IC ：DCDC Converter IC, LDO, PMIC etc.
⇒Low Inductance(Low EMI), Low Resistance

for Automotive Fsw;2MHz↑、Wettable flank

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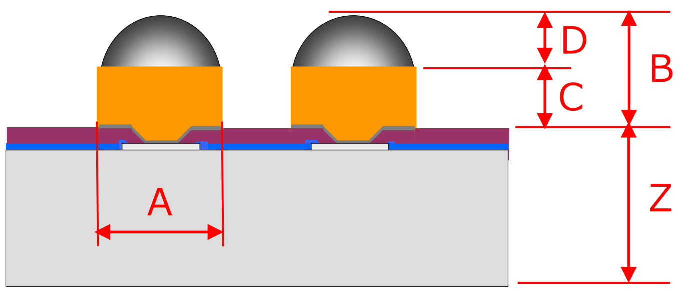
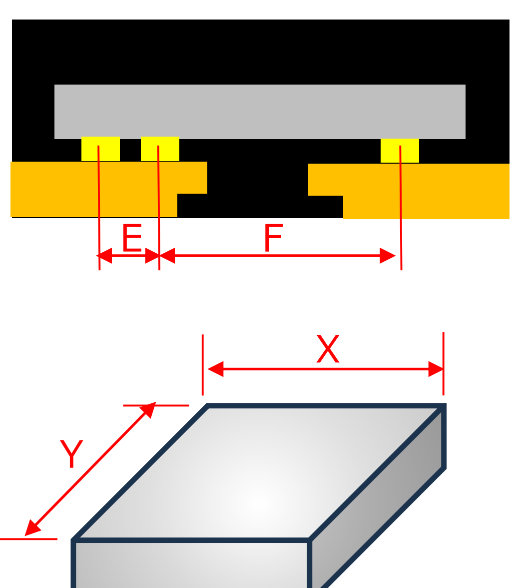
Flip Chip QFN with Cu-pillar

Recommended Design Gide





Items		Symbol	Specification
Wafer diameter		—	8inch＜Option：6inch＞
Cu-Pillar diameter		A	ϕ80μm or ϕ120μm
Cu-pillar height		B	75μm
Cu height		C	50μm
Solder bump height		D	25μm
Cu-Pillar pitch	Same inner lead	E	A=ϕ80μm ：318μmMIN A=ϕ120μm ：358μmMIN
	Different inner lead	F	500μmMIN
Scribe width		—	80μmMIN
Chip size X		X	0.95～1.60mm
Chip size Y		Y	1.35～2.60mm
Chip thickness		Z	200μm
Wafer material		—	Si

※If the above specifications do not meet your needs, please contact us and we will consider your request.

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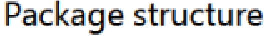
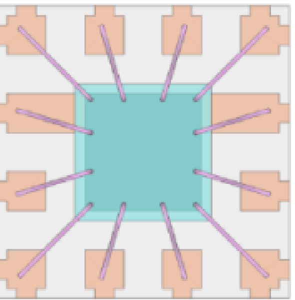
Flip Chip QFN with Cu-pillar

Advantage : Miniaturization and High functionality

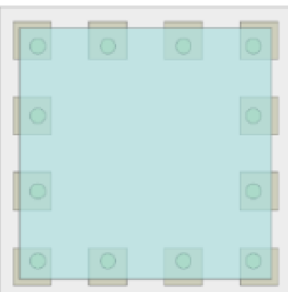
No.	①	②	③
Package size	1.5mm SQ	1.5mm SQ	2.2mm SQ
Chip size	1.33mm SQ	0.7mm SQ	1.33mm SQ
Package Structure	QFN Flip chip	QFN wire	

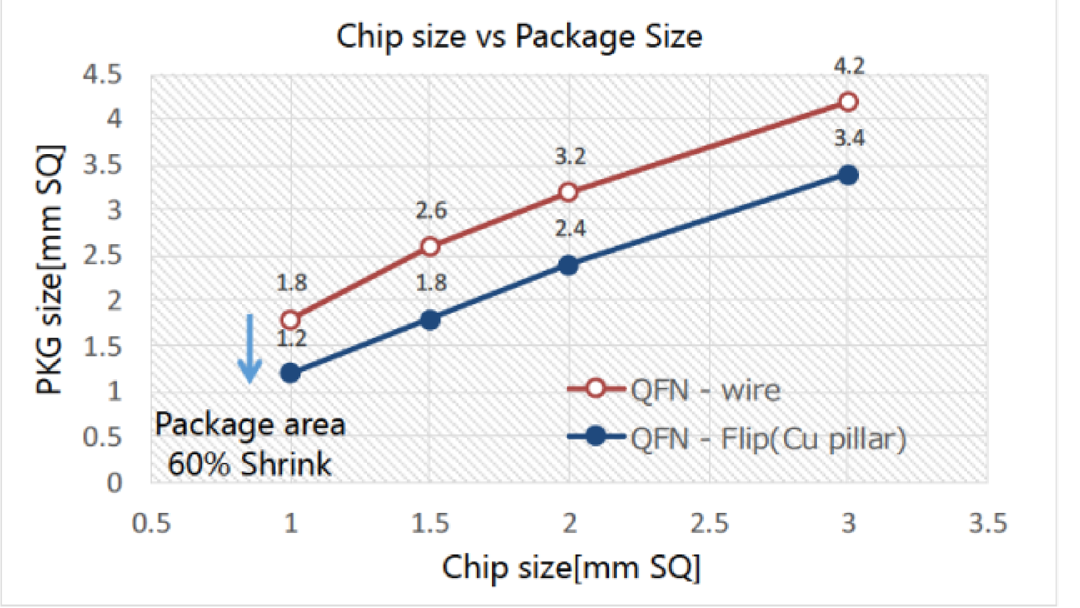


Wire type



Flip chip type





Expected to be Miniaturization and highly functional (large chip size can be installed)

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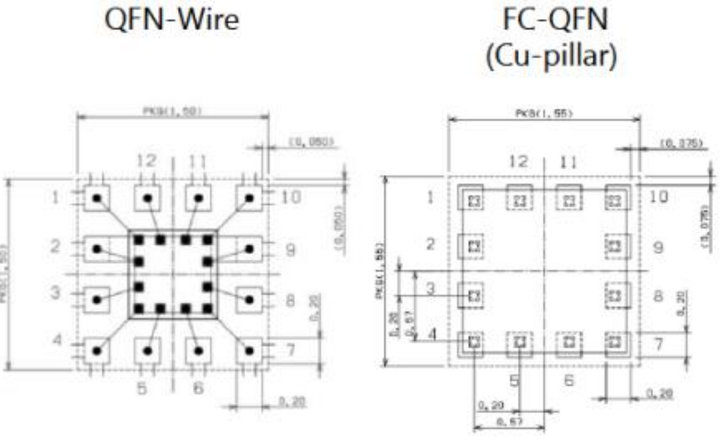
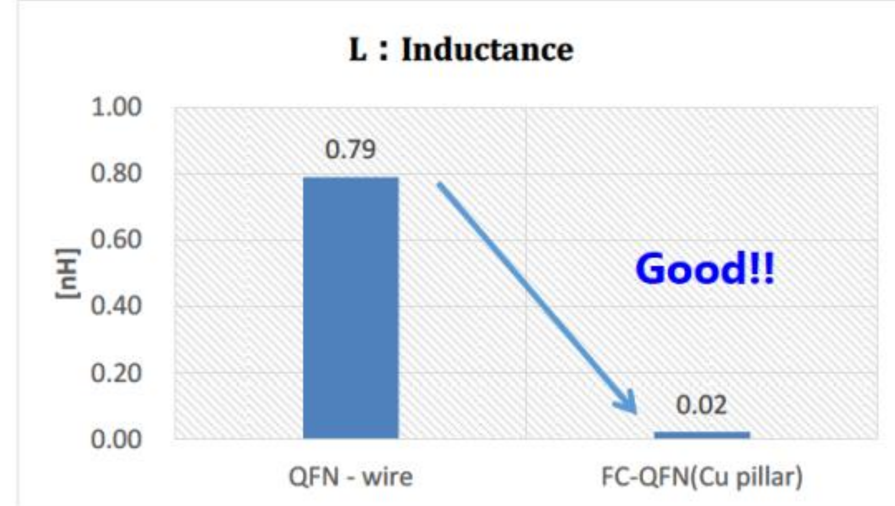
Flip Chip QFN with Cu-pillar

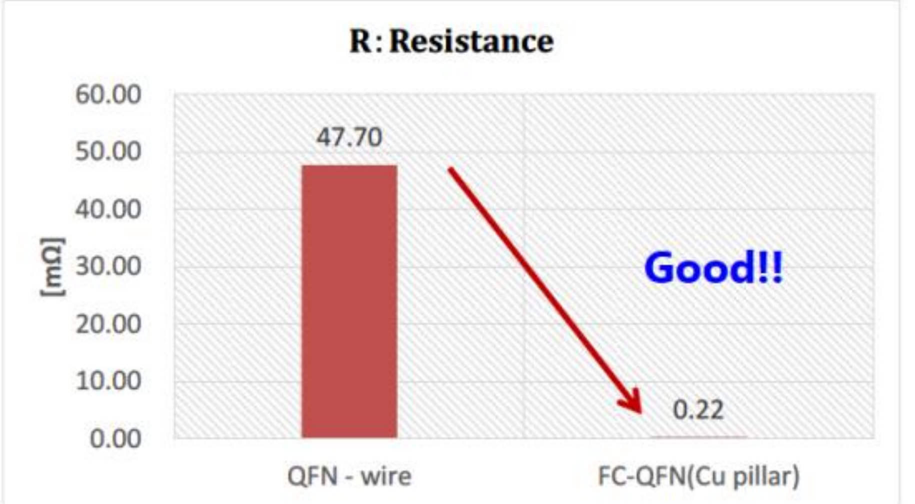
Advantage : Low Electrical Parasitic properties

Electrical Parasitics Comparision (Per one)

	QFN - wire	FC-QFN(Cu pillar)
Package size [mm]	1.5mmSQ	1.5mmSQ
Chip size [mm]	0.70×0.70	1.33×1.33
Lead frame thickness	Cu 0.125mmt	Cu 0.125mmt
Internal wiring	Au wireΦ23μm	Cu pillarΦ80μm/Height50μm
Terminal size	0.2×0.2mm	0.2×0.2mm
L : Inductance [nH]	0.79	0.02
R : Resistance [mΩ]	47.70	0.22







Flip chip QFN package can achieve **Low Inductance** and Low Resistance.
Expected to improve ripple in DC-DC converter IC.

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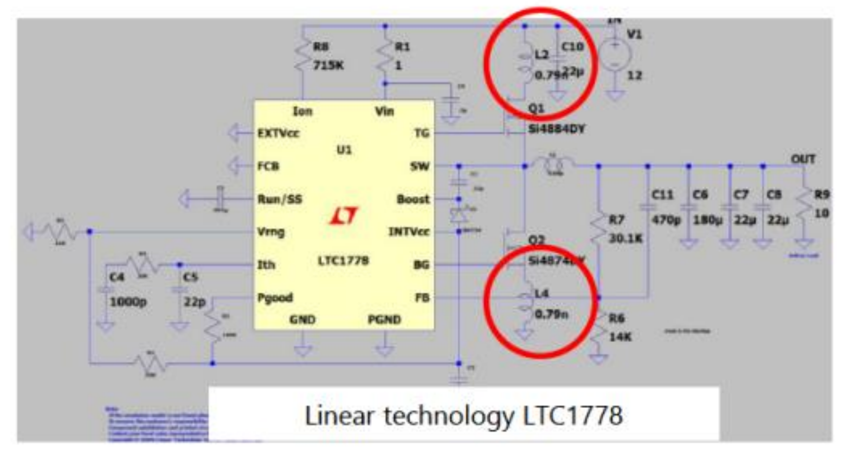
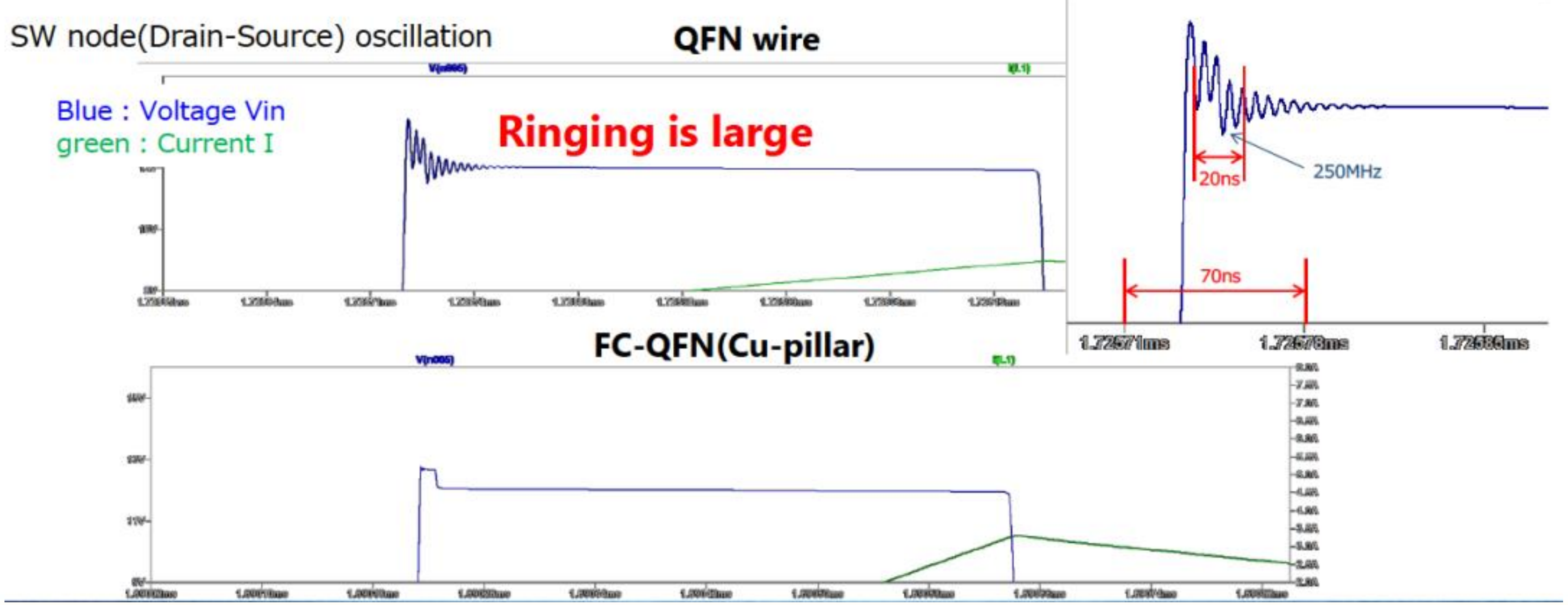
Flip Chip QFN with Cu-pillar



Added parasitic Inductance

QFN wire：L=0.79nH
FC-QFN(Cu-pillar)：L=0.02nH
@frequency:500kHz



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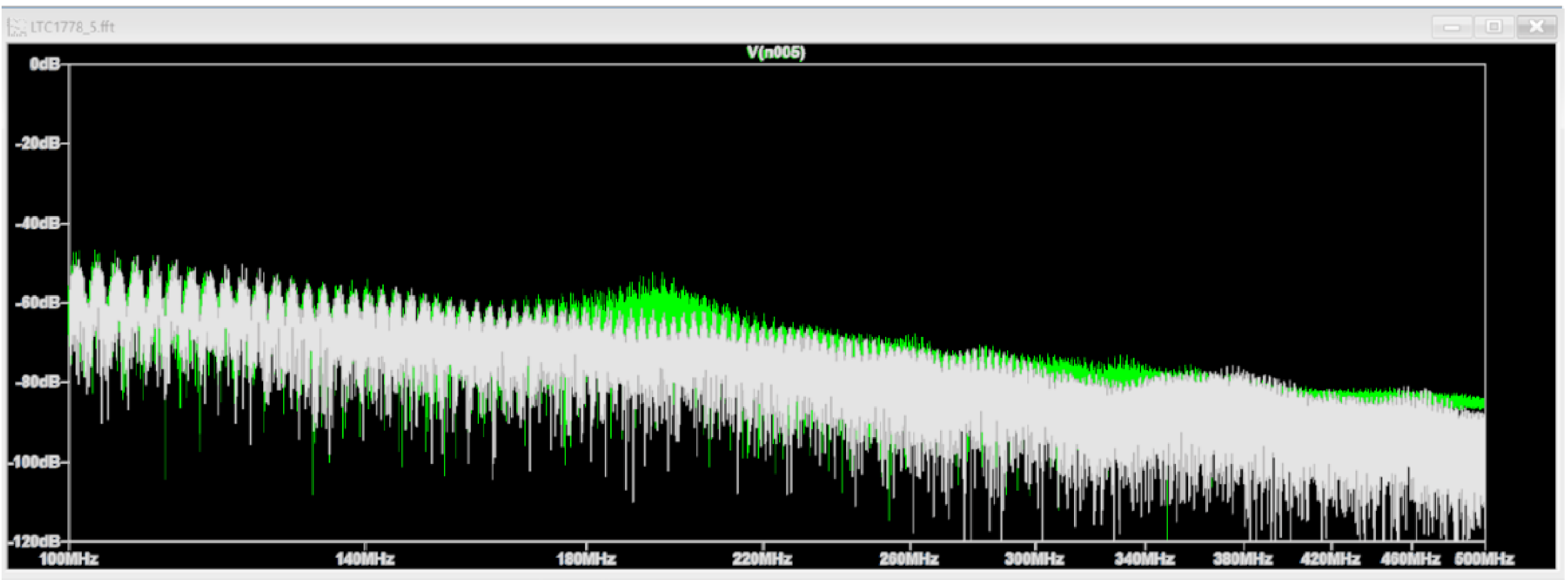
Flip Chip QFN with Cu-pillar

LTSpice @ Step down DC-DC Converter IC

FFT Output frequency analysis

QFN wire 0.79nH(green)

FC-QFN 0.02nH(gray)



EMI improvement is about 10 dB@200MHz.
EMI improvement of 3 to 5 dB above 220MHz.

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Flip Chip QFN with Cu-pillar

Thermal resistance Simulation(steady state)

		QFN wire A	QFN wire B	QFN Flip chip
Package structure				
Package size		1.5mm SQ	2.2mm SQ	1.5mm SQ
Chip size		0.7mm SQ	1.33mm SQ	1.33mm SQ
4-layer board (No via)	Thermal resistance [℃/W]	153	103	88.4
	PD [W]	0.65	0.97	1.13

※ PD : Tj=125℃, Ta=25℃

- Boundary condition
  - Atmospheric temperature : 0℃ ※Assumption: No radiant heat dissipation
  - Calorific value : 1W （The heat generation density is set uniformly on the chip surface.）
  - Heat transfer coefficient : 10 W/(m^2℃) ※Natural air cooling
- Mounting board
  - 1/2 symmetry (JEDEC51-7, 4-layer board 38.1x114.3xt1.6)

The heat generation density is small due to the large chip area of FCQFN

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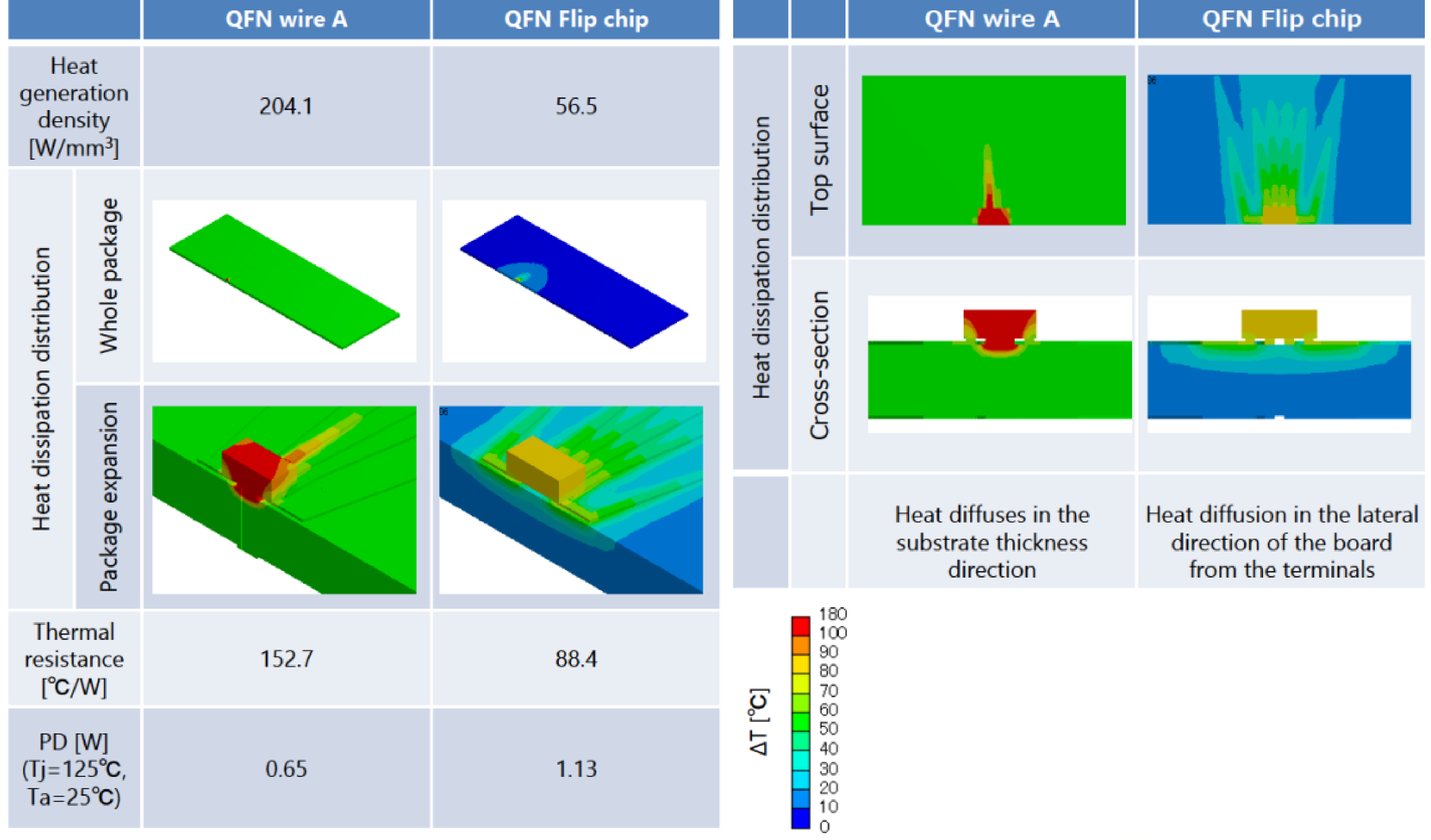
Flip Chip QFN with Cu-pillar

Thermal resistance Simulation(steady state)



		QFN wire A	QFN Flip chip
Heat generation density [W/mm³]		204.1	56.5
Heat dissipation distribution	Whole package		
	Package expansion		
Thermal resistance [℃/W]		152.7	88.4
PD [W] (Tj=125℃, Ta=25℃)		0.65	1.13

		QFN wire A	QFN Flip chip
Heat dissipation distribution	Top surface		
	Cross-section		
		Heat diffuses in the substrate thickness direction	Heat diffusion in the lateral direction of the board from the terminals

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