

Introduction of FOLP[®] technology

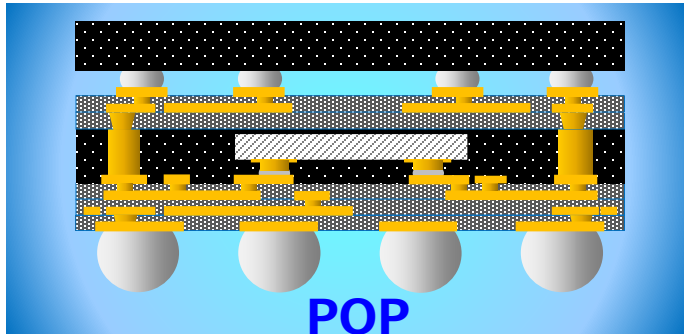
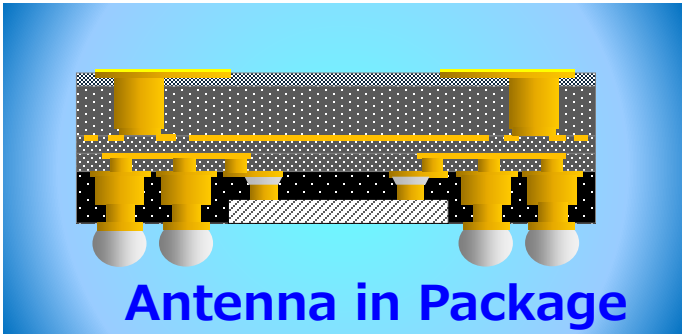
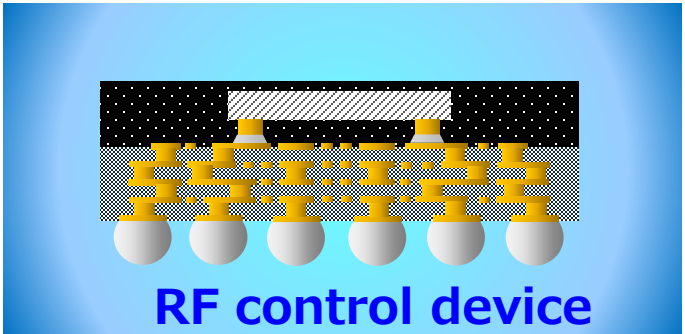
FOLP[®] (Fan-Out Laminate Package)/ FOPLP

High frequency application

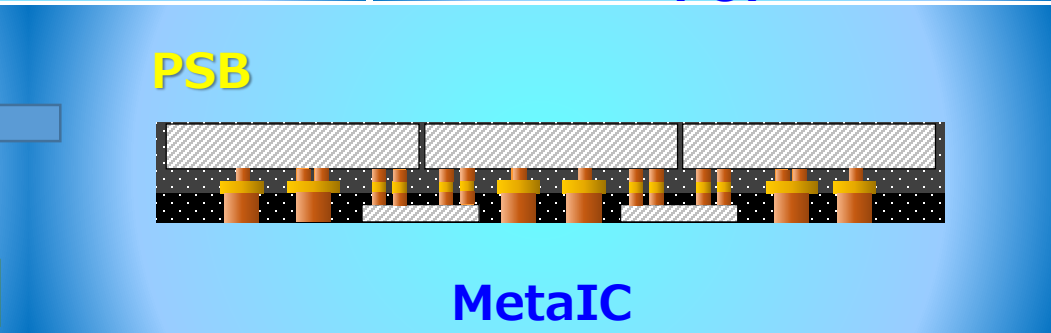
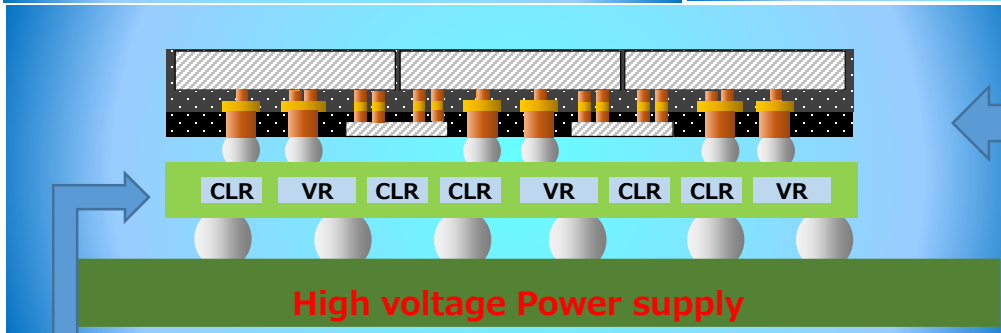
Logic application (Chiplet integration)

Power Module application

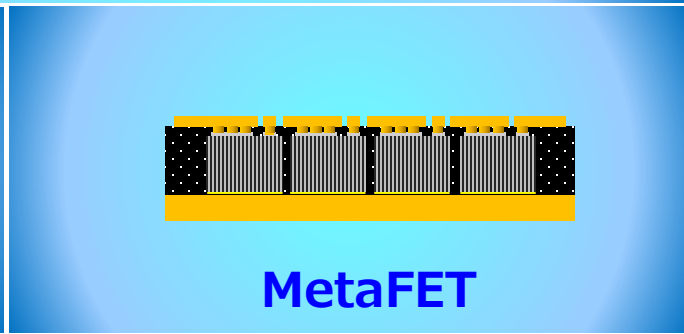
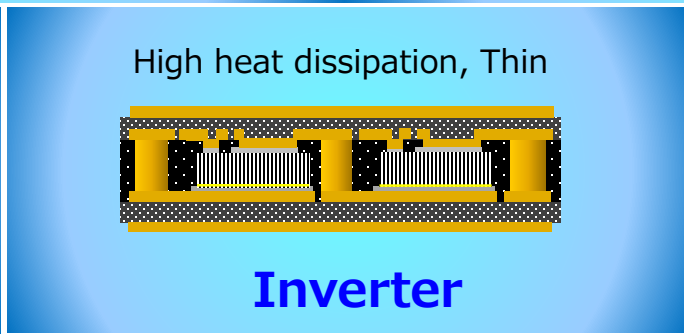
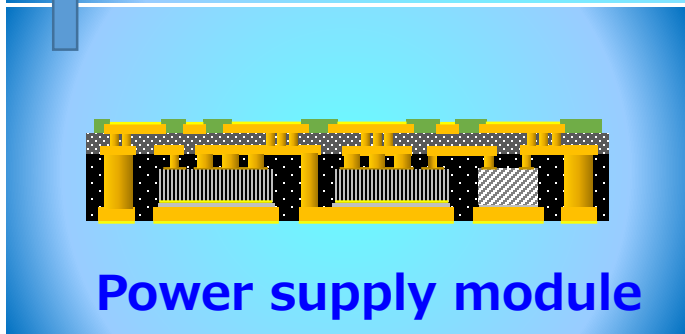
High frequency application



Logic application (Chiplet integration)



Power Module application

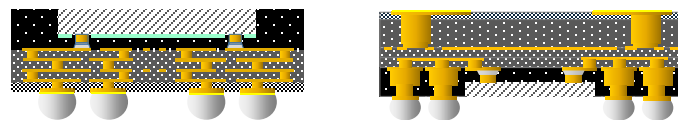


FOLP[®] Technology Direction (Trend)

RDL-first (fine pitch/multi-layer)

High Frequency

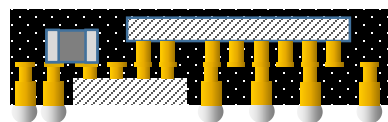
Multi-Layer, 3 D FOLP[®]



High Via connection reliability
Deep plugged Via
Low RF signal loss
(Low Df material)

Logic

Fine pitch FOLP[®] Chiplet



Fine pillar pitch
Fine Line/Space
High yield (Simple structure)

Chip-first (high heat dissipation/low resistance)

Power Module

Thinner , Heat dissipation FOLP[®]

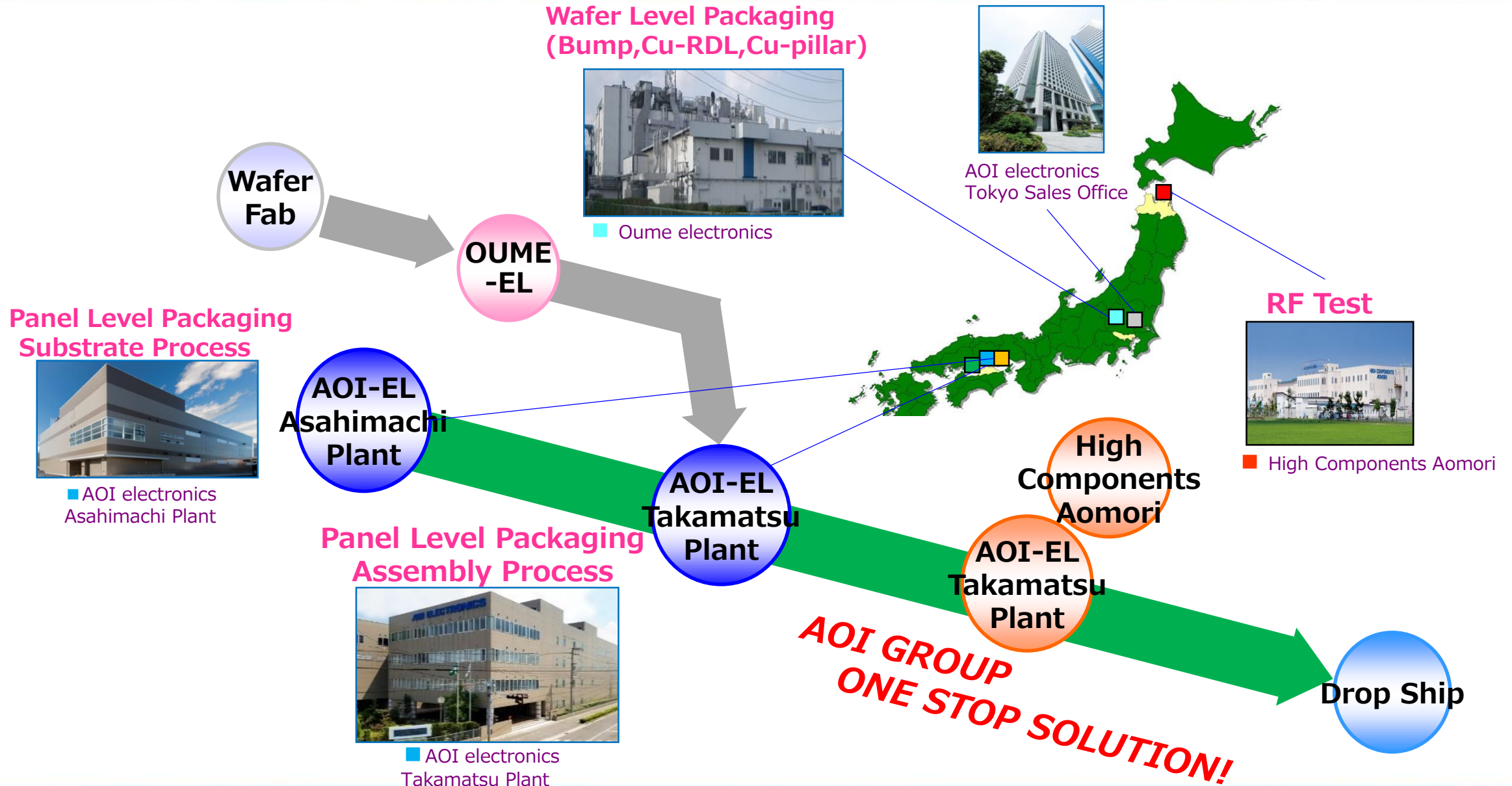


Low electrical resistance wiring
Low inductance wiring
High heat dissipation
(High thermal conductive material)
High operation temperature
(High Tg material)

Warpage control



FOLP[®] Production Platform



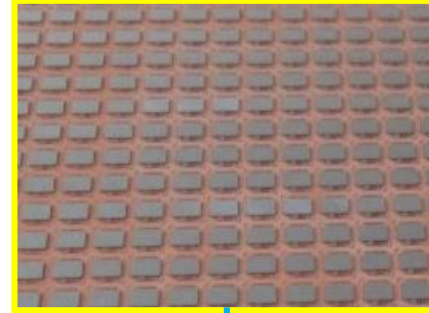
FOLP[®] *for High Frequency application*

FOLP[®] Elemental technology (1)

RF controller

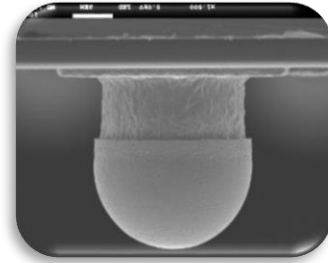
FC-Bonding

Si, SiGe, GaN, GaAs, Others (100 μ mt)

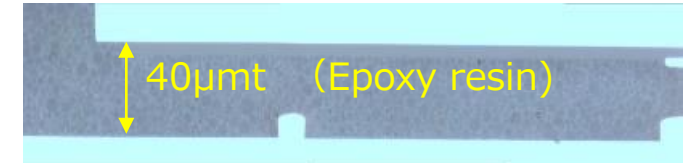
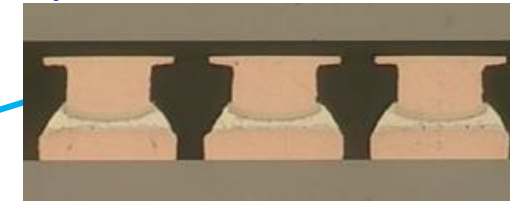


Cu Pillar Bump

40 μ m ~ Pitch

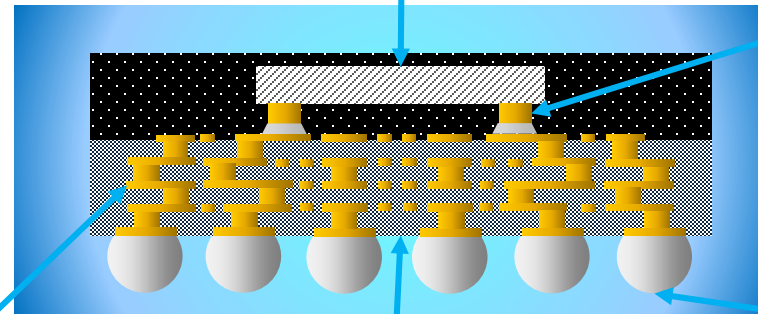
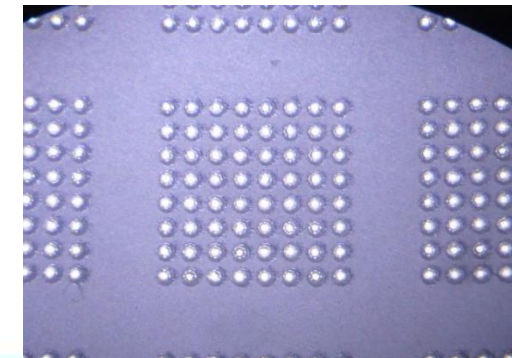


C2 bonding & encapsulation



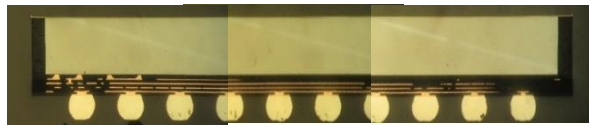
Solder Bump

SAC, SACN, SACNBI Others

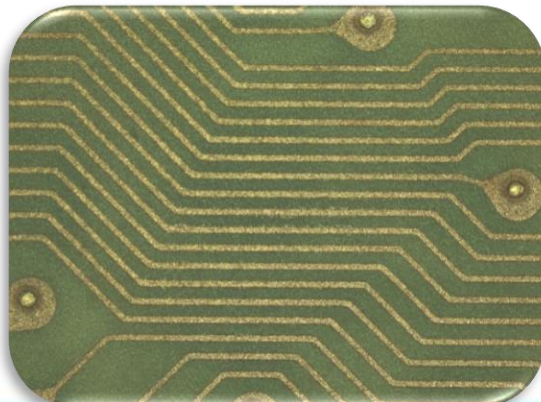


Low stress insulator

CTE (25~150 $^{\circ}$ C) 14ppm
Young's modulus 10GPa



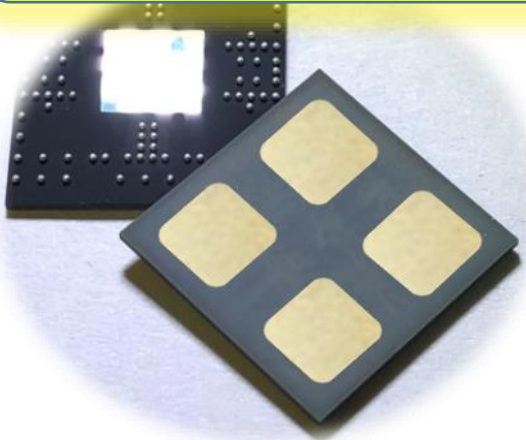
Fine Pitch RDL (Line=10 μ m)
(Max 5 Layers in MP, 8 Layers in trial)



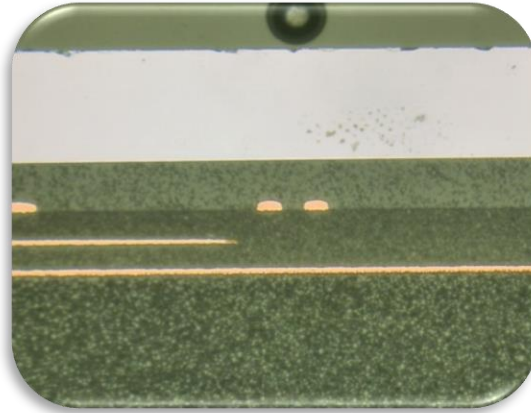
FOLP[®] Elemental technology (2)

Applied Model

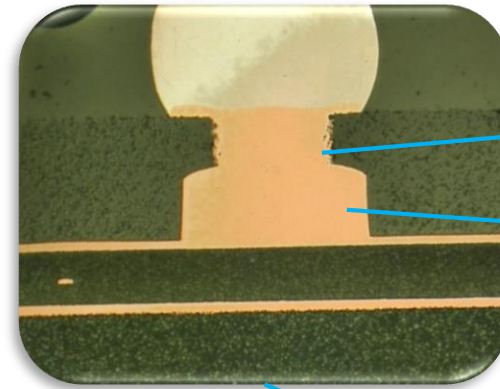
AiP Case



Backside Grinding



ToM(Terminal on Mold)



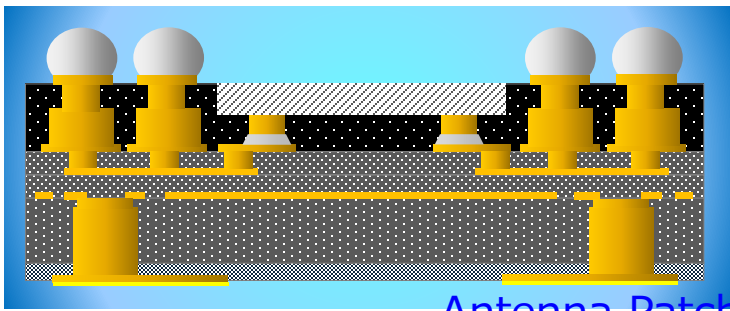
TRV(Through Resin Via)
+
Cu Post



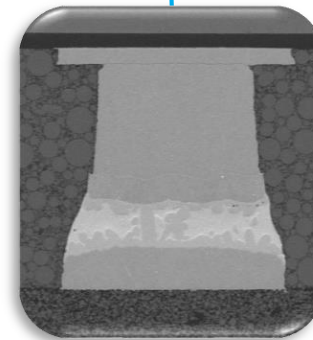
Resin

Accurate Via
alignment
on antenna

Low Df Isolation
(0.002 ~)



Antenna Patch



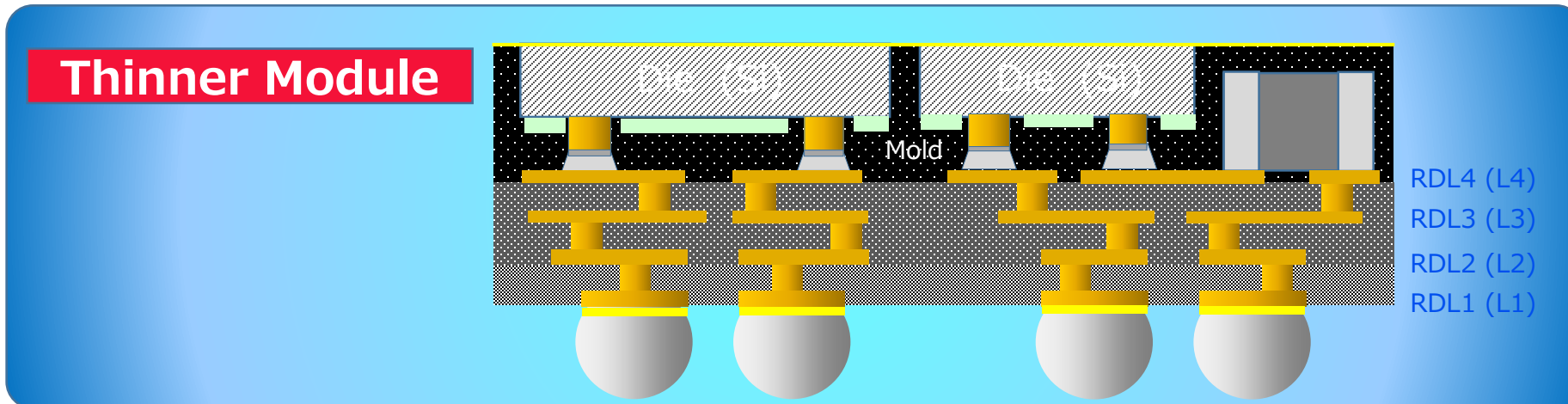
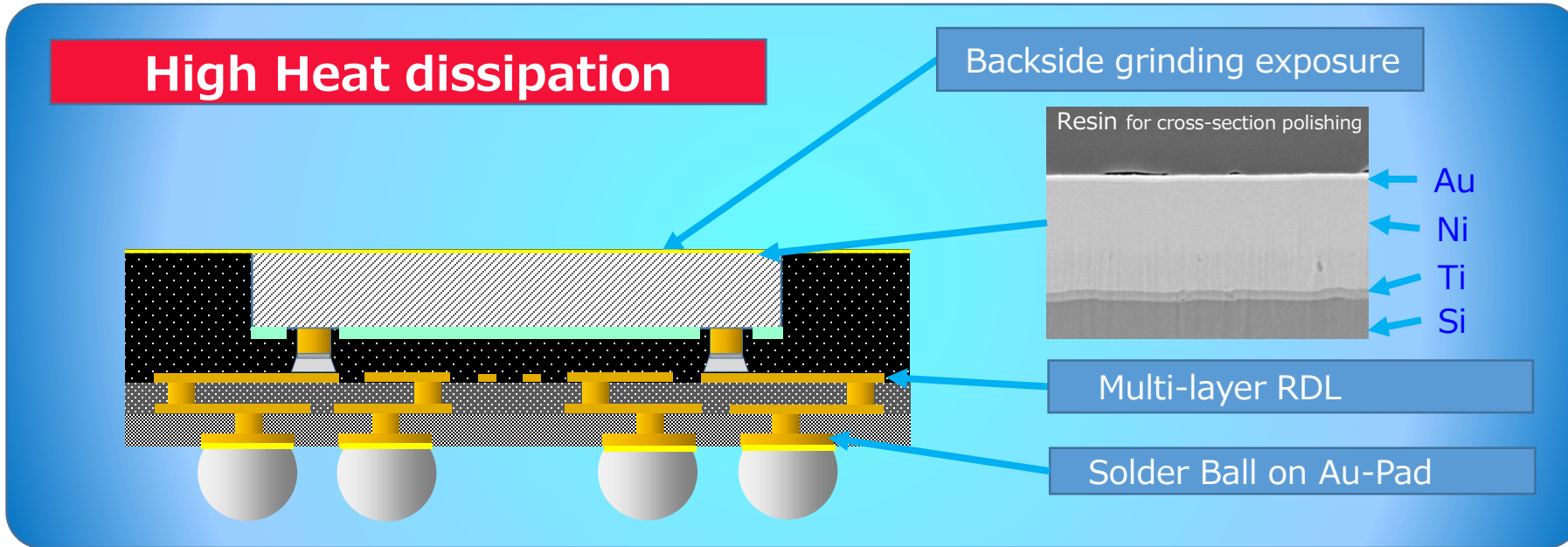
C2 bonding



200~400µm

PLUG(Plugged Via)

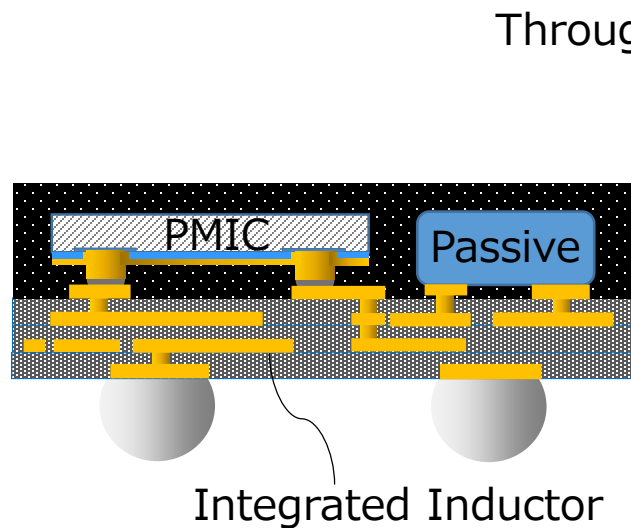
Active+Passive device FOLP® Module



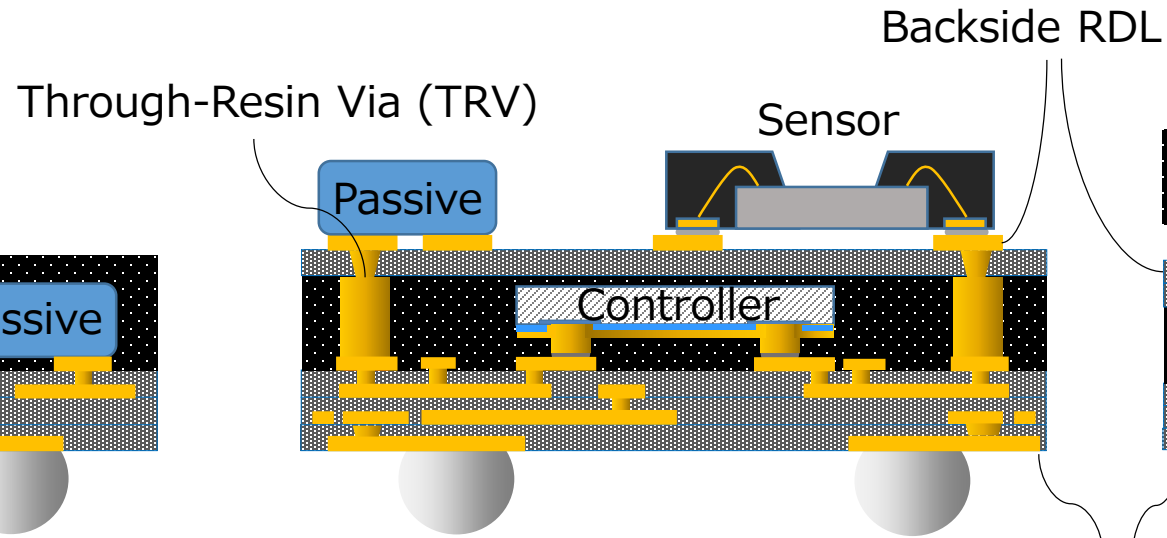
Flexible Structural Design for Various Applications

Epoxy-based RDL-first process enables flexible structural design for various applications.

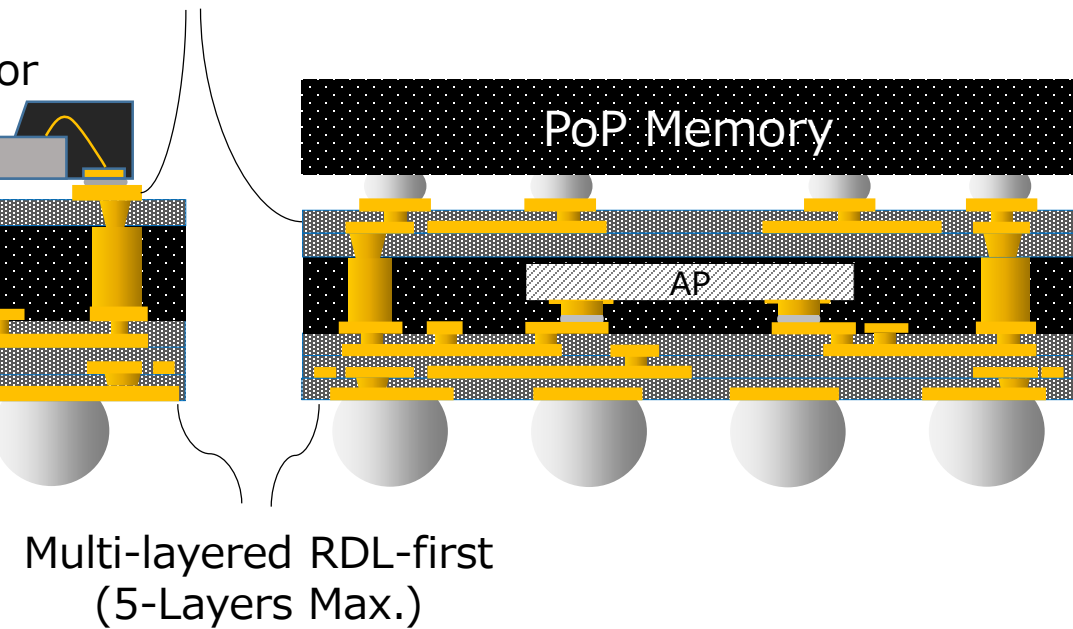
Power Management



Sensor Module



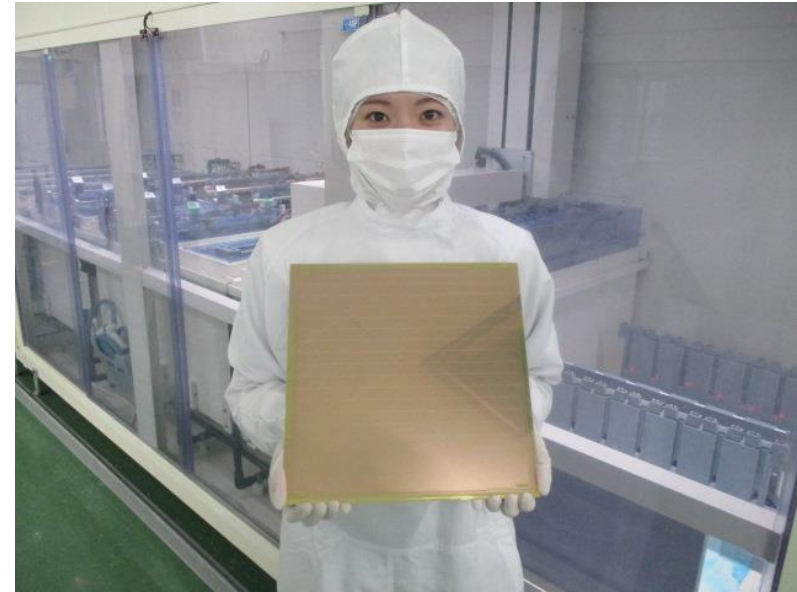
Mobile Processor



Multi-layered RDL-first
(5-Layers Max.)

FOLP[®] Process Advantage

- 1.High Yield** : KG-RDL + KGD Combination
- 2.Short cycle time** : Horizontal specialization Process
Wafer Bumping & Substrate (RDL) Process
+Assembly + Test Process
- 3.Cost effective** : Mechanical de-bonding system
MUF(mold under fill) Process
300mm Sq. Panel
- 4.One stop solution in AOI electronics Group.**
- 5.High Reliability** : Modified Epoxy Resin (High Tg, Low Warpage)
Solder materials of various composition
- 6.High Performance** : Good design flexibility
Low Dk,Df substrate materials for RF devices(5G⇒6 G)
High heat dissipation, Low impedance for power IC



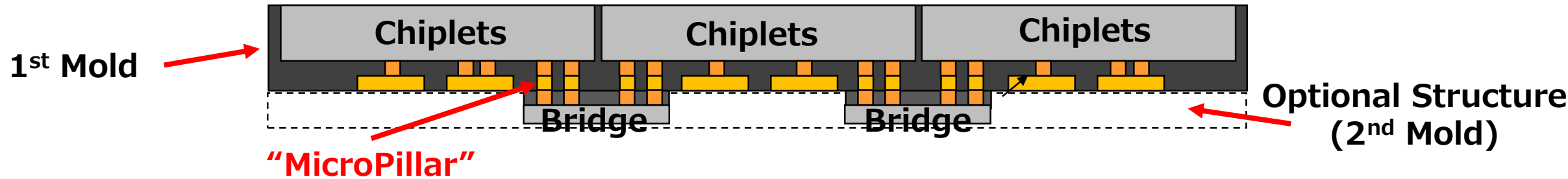
FOLP® *for Logic application
(Chiplet integration)*

Conventional Chiplet Integration using “Interposer”

Technology	Si interposer	RDL interposer	Embedded Bridge interposer
Pros	<ul style="list-style-type: none">✓ Technology maturity	<ul style="list-style-type: none">✓ Excellent electrical characteristics✓ Relatively low cost	<ul style="list-style-type: none">✓ Excellent electrical characteristics✓ L/S selectability
Cons	<ul style="list-style-type: none">✓ Electrical characteristics✓ High cost✓ Size limitation (Wafer only)	<ul style="list-style-type: none">✓ Feasibility of fine L/S at panel-level✓ Need bridge assist in case of sub-micron L/S	<ul style="list-style-type: none">✓ Complicated process and structure✓ High cost✓ Limited connection Pitch between bridge and chiplets

"Pillar Suspended Bridge"

AOI proposal



- High positioning accuracy of bridges
- ✓ Face-Down bonder ($\sim 1 \mu\text{m}$)
- ✓ Die shift is avoided by fixing with Micro Pillars
- ✓ Not affected by variations in chip thickness
- Simple process & material handling scheme

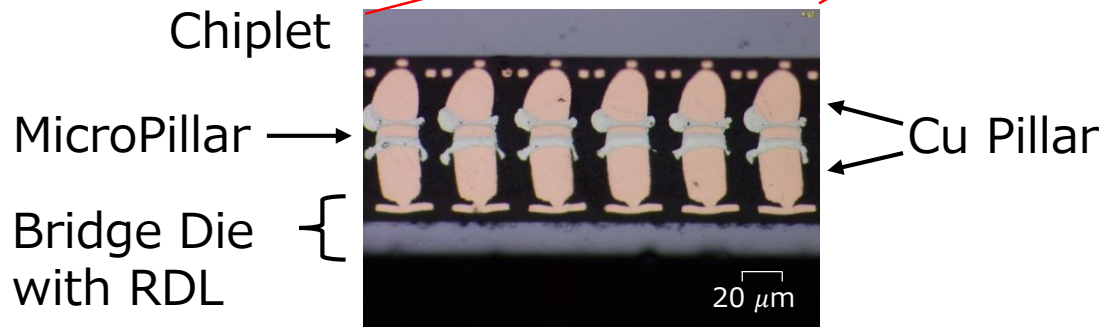
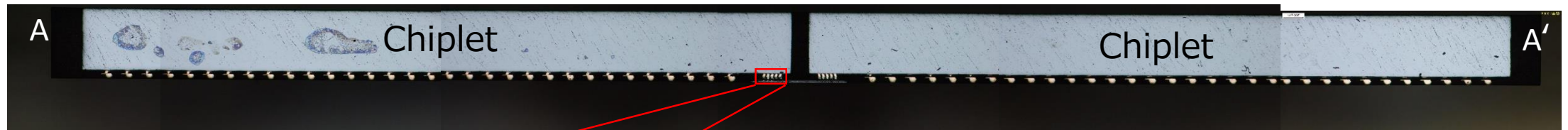
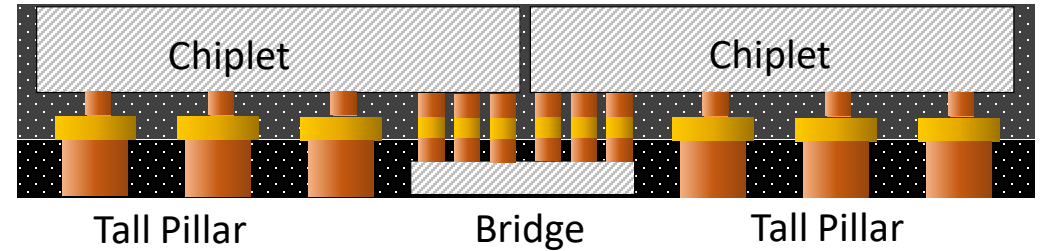
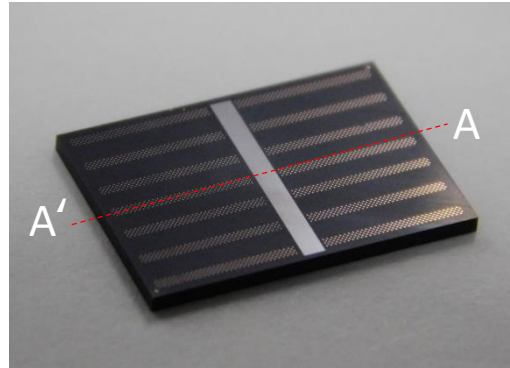
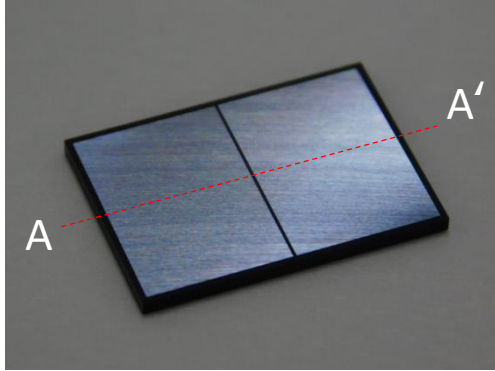


Excellent scalability

- ✓ *Expandability to panel-level processing*
- ✓ *Finer connection pitch for bridge ($< 20 \mu\text{m}$)*

Internal Structure of Proof-of-Concept Sample

Die-to-Die interconnect by 20 μm thick Bridge



- MES2022 “A Simple Die-to-Die Bridge Architecture”
“Evaluation with the Best Paper Award”
- IMAPS 2022 “Chiplet Integration by Die-to-Die Pillar-Suspended Bridge”
- ECTC 2023 “A Novel Chiplet Integration Architecture Employing Pillar-Suspended Bridge with Polymer Fine-Via Interconnect”

FOLP[®] *for Power Module application*

Background

■ Applications : Power Supply System



Source : NTT Corporation



Source : TOYOTA corporation

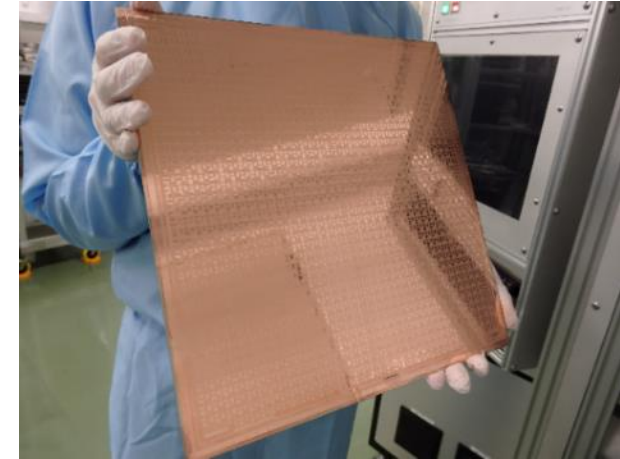
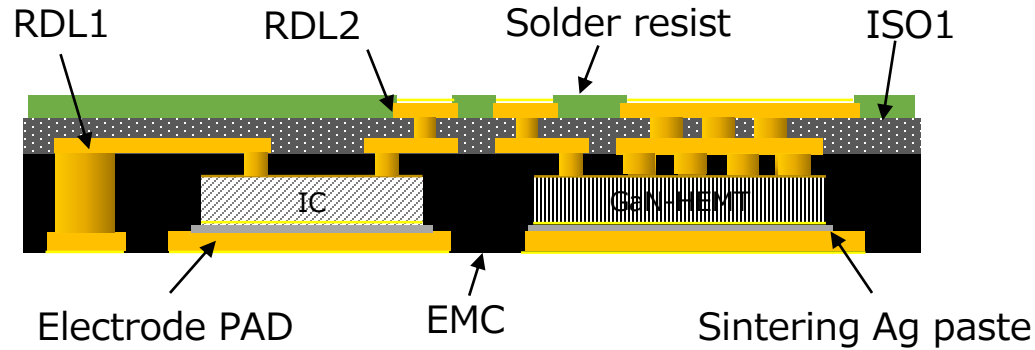
- ✓ Data centers and various power supply equipment shift from 12V to 48V systems.
- ✓ As power supply output current increasing, wiring resistance is a big issue about power distribution loss.
- ✓ Placing the power supply near the processor (CPU/GPU) will be an important for power integrity.
- ✓ Chip-embedded packages (PoP/CoP/3D-SiP) can shrink size and increase current density.

According to Texas Instruments 's white paper, they have brought an average module size reduction of 25 percent annually.

Source : U. Chaudhry et al, SiP Power Modules White Paper "Powerful solutions come in small packages", Texas Instruments, page2

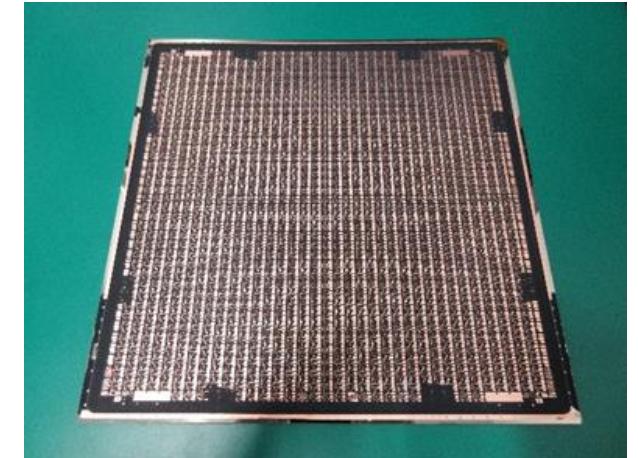
Introduction of Our Coreless Chip Embedded Technology

AOI's new approach of *Ultra thinner, Higher heat dissipation* chip embedded technology in analog and power solutions.



Features of this concept

- Unique Coreless structure
 - ① All Cu plating
 - ② Chip embedded method
 - ③ Power customized fan-out processes
- Excellent thermal property
- SoC-like extra thin packages

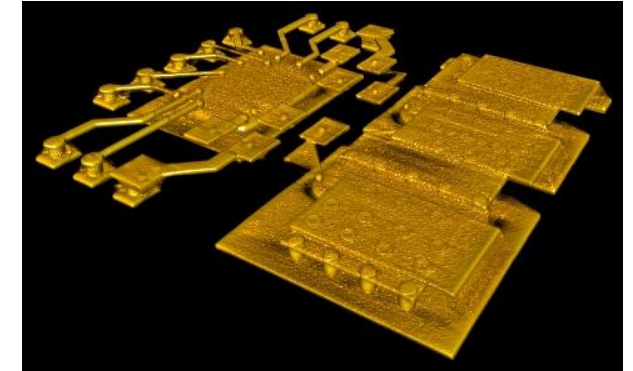
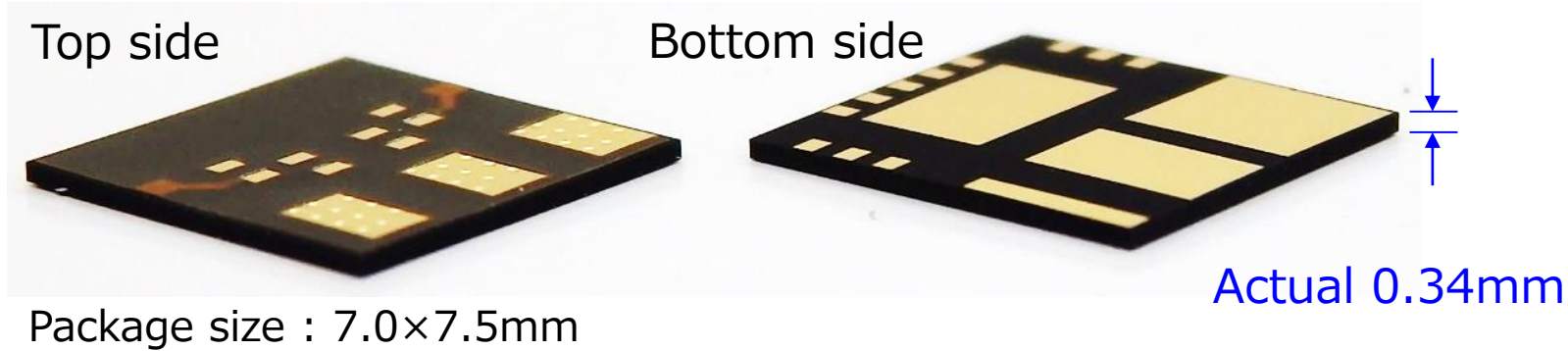


Trial production and evaluations for a Prototype

■ Prototyped package

New Coreless chip embedded module package

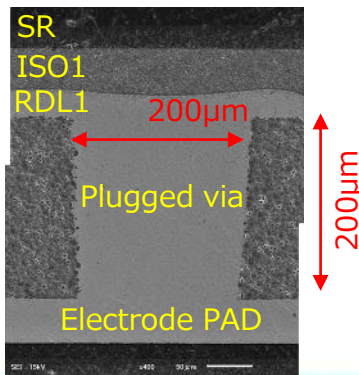
*X-ray CT 3D image
(Internal structure)*



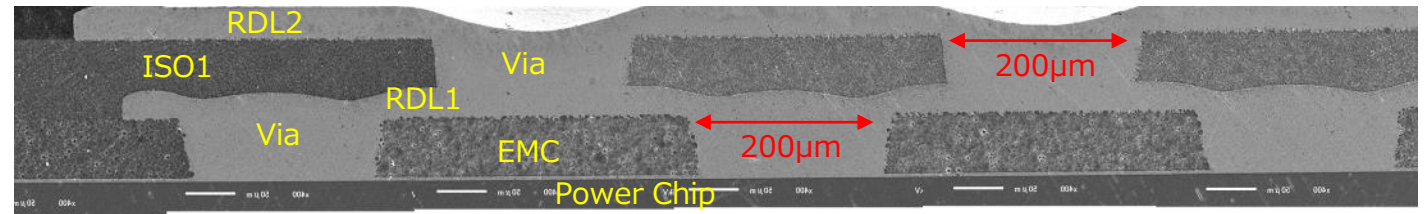
Actual Cross section



Cu plugged via


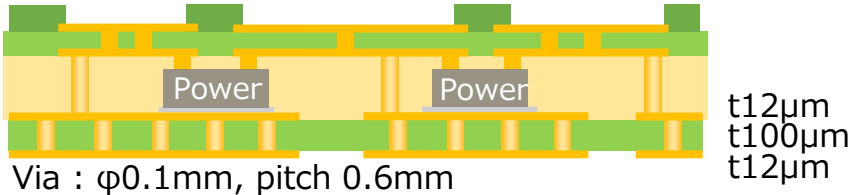
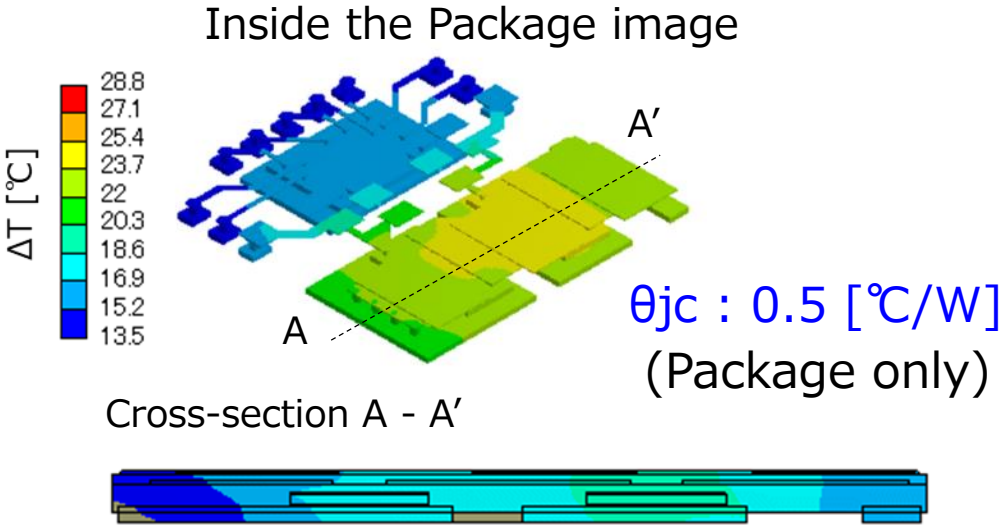
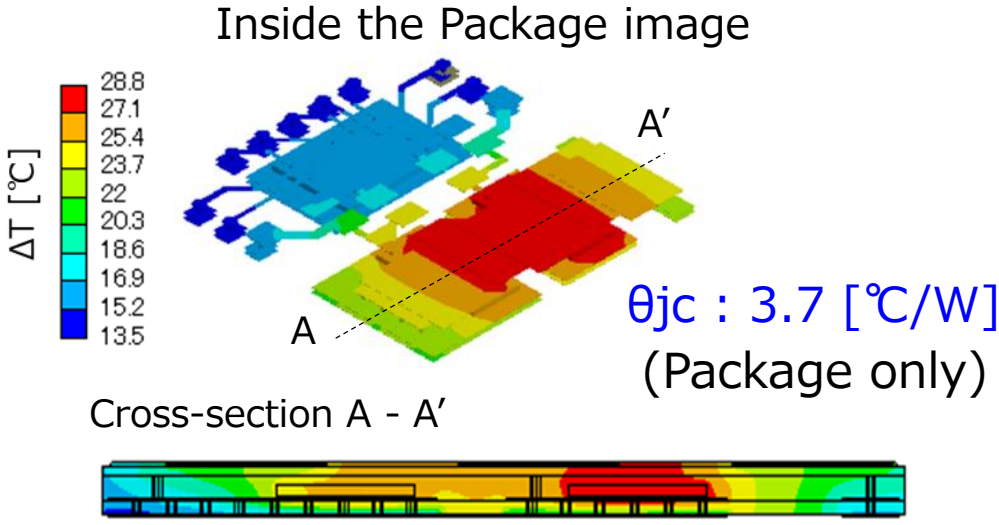


Direct Cu plating connection of power chips



Thermal Resistance Simulation with Our Concept Package

■ Simulation result

	Our Concept package	Prepreg package (assumption)
Structure	 <p>t50µm</p>	 <p>t12µm t100µm t12µm Via : φ0.1mm, pitch 0.6mm</p>
Thermal simulation result	<p>Inside the Package image</p>  <p>ΔT [°C]</p> <p>28.8 27.1 25.4 23.7 22 20.3 18.6 16.9 15.2 13.5</p> <p>θ_{jc} : 0.5 [°C/W] (Package only)</p> <p>Cross-section A - A'</p>	<p>Inside the Package image</p>  <p>ΔT [°C]</p> <p>28.8 27.1 25.4 23.7 22 20.3 18.6 16.9 15.2 13.5</p> <p>θ_{jc} : 3.7 [°C/W] (Package only)</p> <p>Cross-section A - A'</p>

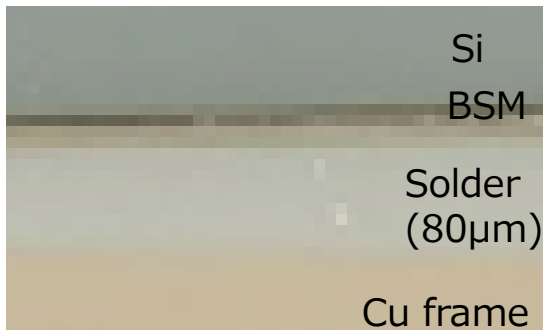
Embedded Multi-Chip in Molded Package

Package structure for Half-Bridge DC/DC converter

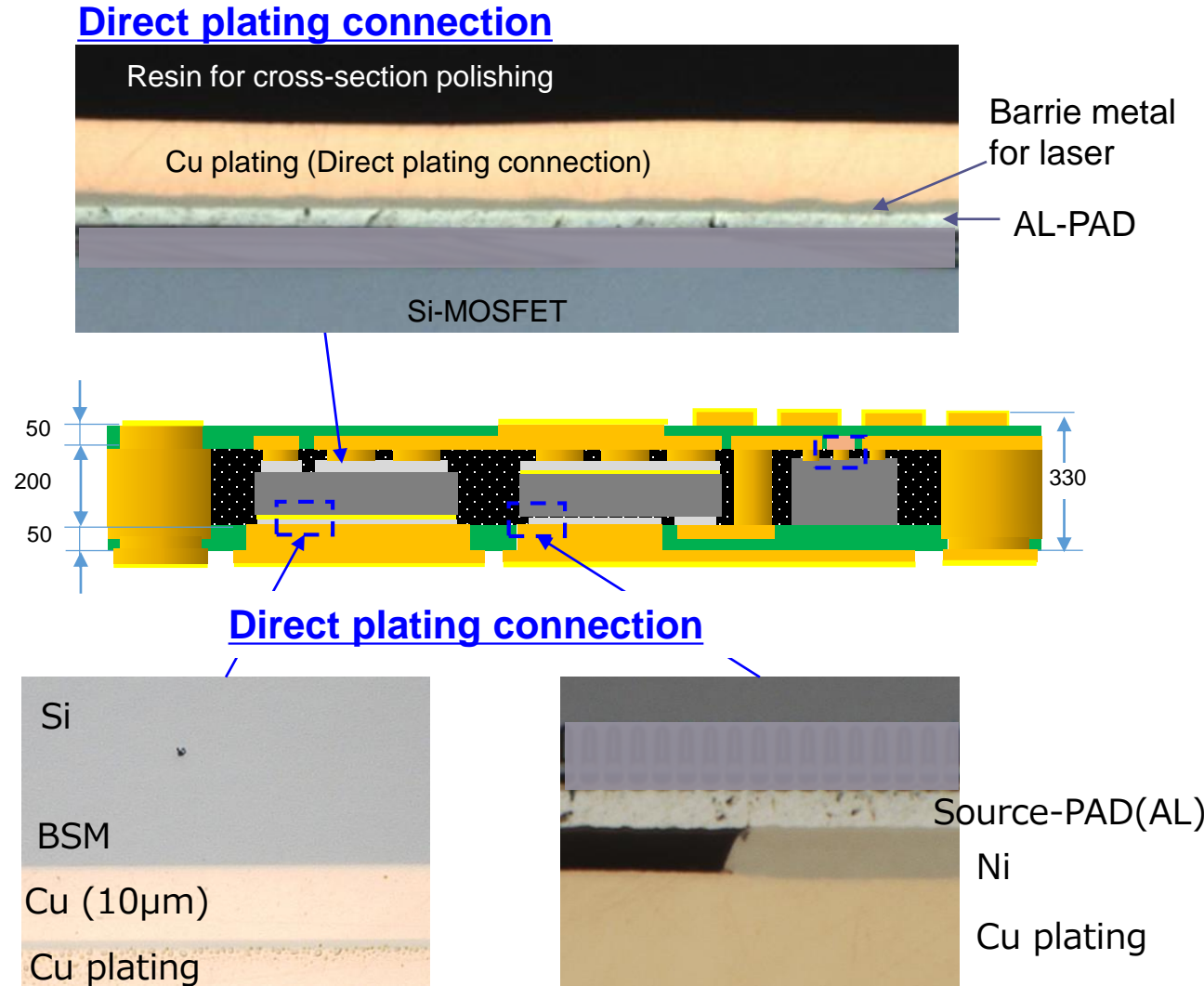
Solderless connect

- ⇒ • Lower impedance
• Lower noise response to high freq. switching

Solder connection



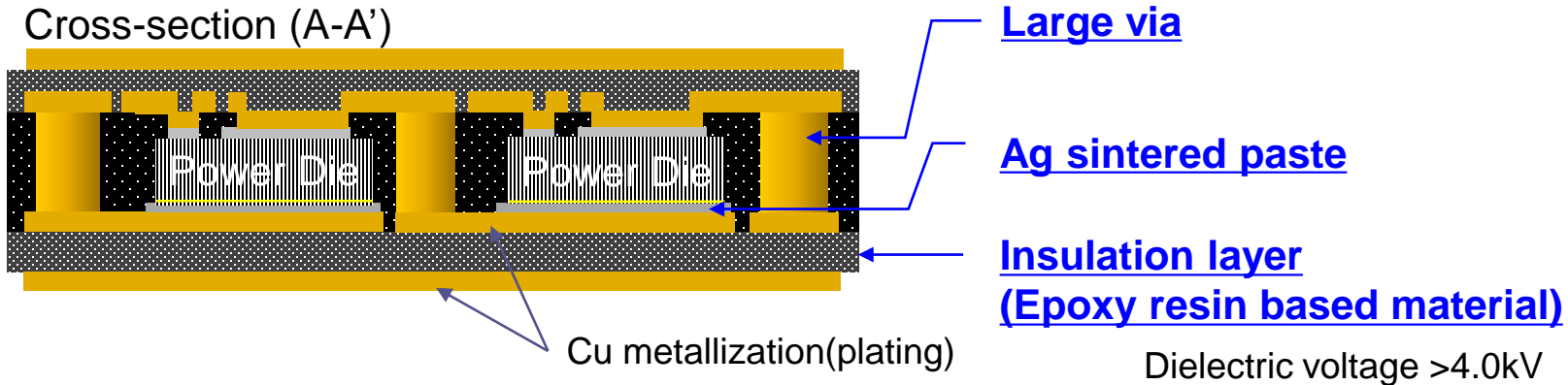
DB material
Electrical conductivity 50times
Thermal conductivity 38times



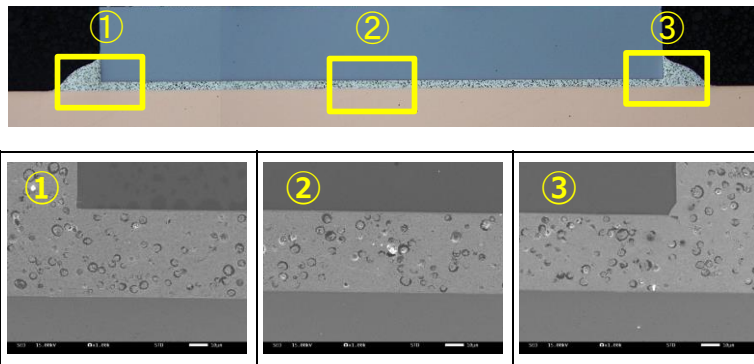
Package structure for Inverter IC module

Embedded power package without DBC substrate

Cross-section (A-A')



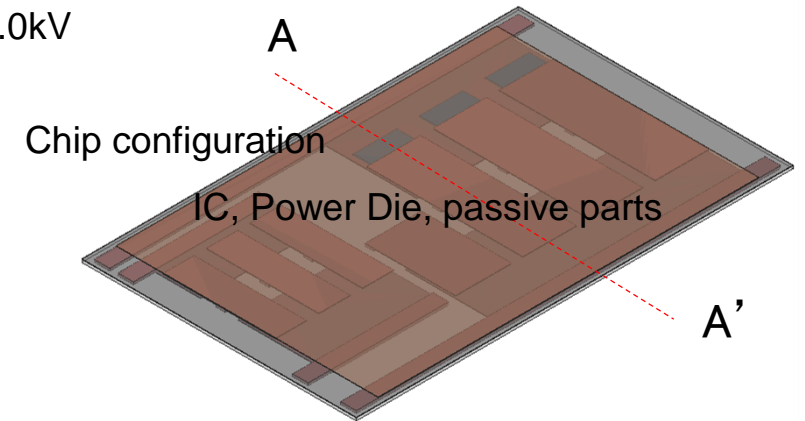
Dielectric voltage >4.0kV



Power die Ag sintered paste

Target ; Si, SiC etc.

3D-MODEL

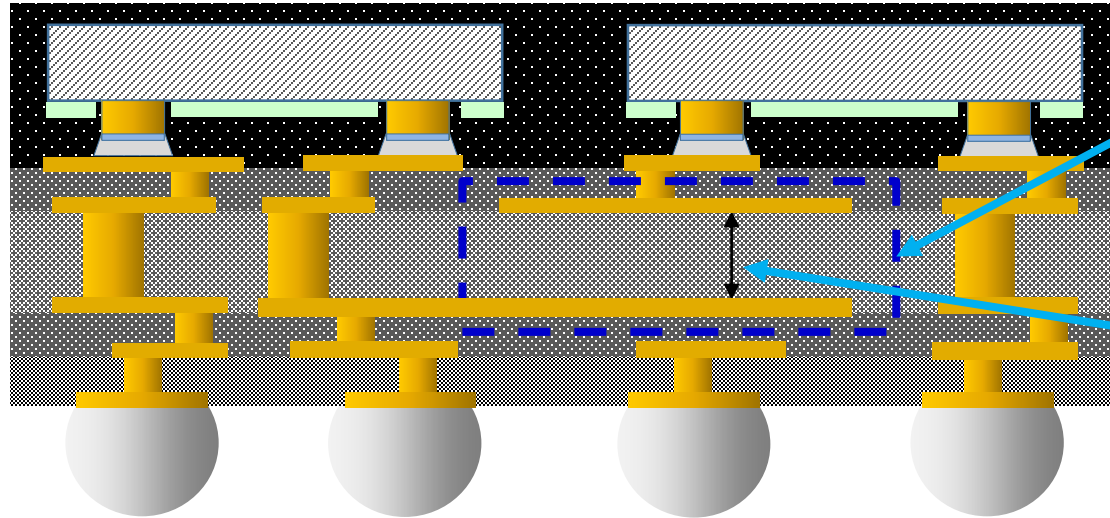


Prototype module

High voltage isolation by FOLP®

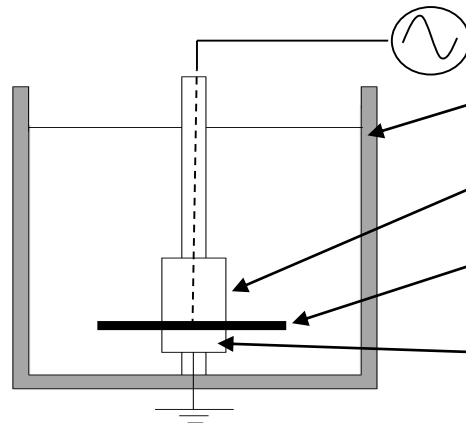
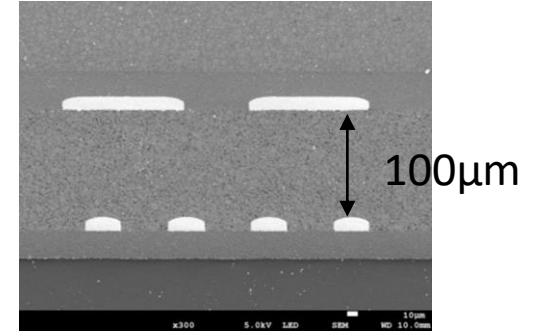
Embedded Coupling Devices

*RDL High Voltage Isolation
for Digital Isolator, Isolation Power supply etc.*



Coupling Device

High Voltage Isolation



Oil bath (Silicon oil)

Upper electrode

Sample

Under electrode

Based on ASTM-D149

Isolation(μm)	kV/mm
100	122.7

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