Introduction of FOLP® technology

FOLP ® (***F****an-****O****ut* ***L****aminate* ***P****ackage)/ FOPLP*

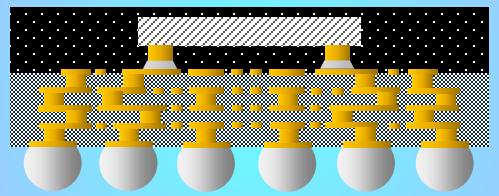
High frequency application

Logic application (Chiplet integration)

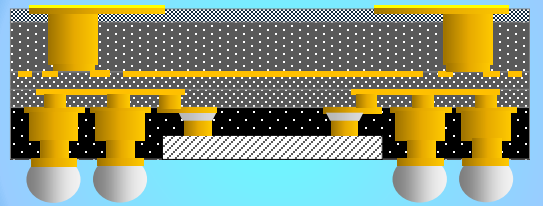
Power Module application

FOLP® Package, Module & Meta-Chip Example

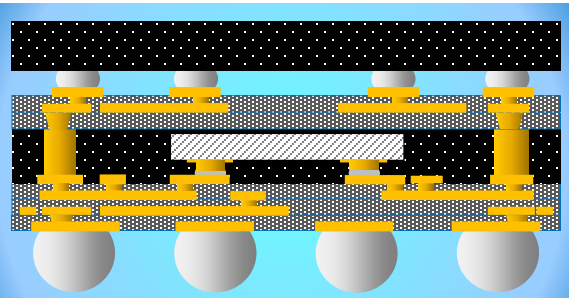
High frequency application



RF control device

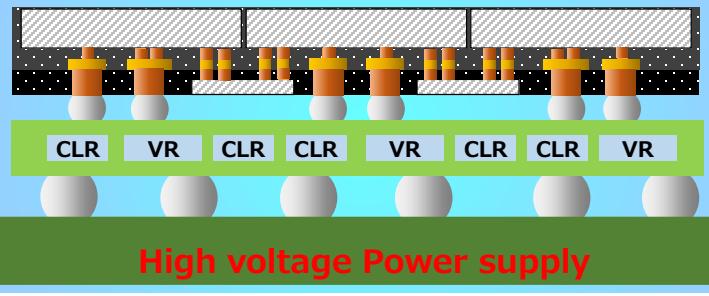


Antenna in Package

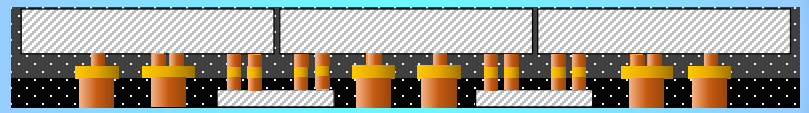


POP

Logic application (Chiplet integration)

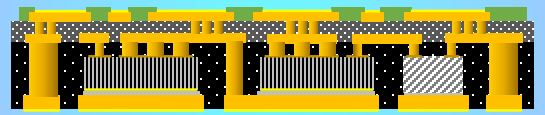


PSB



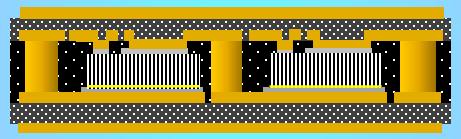
MetaIC

Power Module application

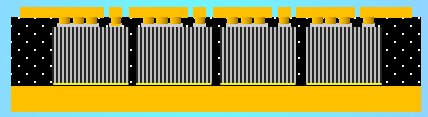


Power supply module

High heat dissipation, Thin



Inverter



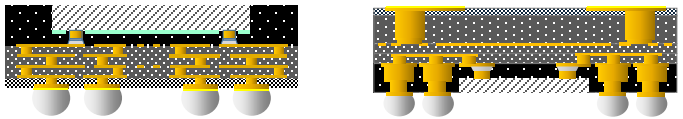
MetaFET

FOLP® Technology Direction (Trend)

RDL-first *(fine pitch/multi-layer)*

High Frequency

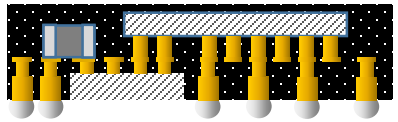
Multi-Layer, 3D FOLP®



High Via connection reliability
Deep plugged Via
Low RF signal loss
(Low Df material)

Logic

Fine pitch FOLP® Chiplet

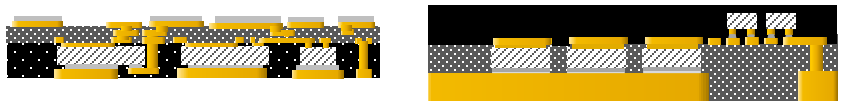


Fine pillar pitch
Fine Line/Space
High yield (Simple structure)

Chip-first *(high heat dissipation/low resistance)*

Power Module

Thinner , Heat dissipation FOLP®



Low electrical resistance wiring
Low inductance wiring
High heat dissipation
(High thermal conductive material)
High operation temperature
(High Tg material)

Warpage control

FOLP® Production Platform

Wafer Level Packaging
(Bump,Cu-RDL,Cu-pillar)

■ Oume electronics

AOI electronics
Tokyo Sales Office

Wafer Fab

OUME -EL

Panel Level Packaging
Substrate Process

■ AOI electronics
Asahimachi Plant

AOI-EL Asahimachi Plant

AOI-EL Takamatsu Plant

RF Test

■ High Components Aomori

High Components Aomori

AOI-EL Takamatsu Plant

Panel Level Packaging
Assembly Process

■ AOI electronics
Takamatsu Plant

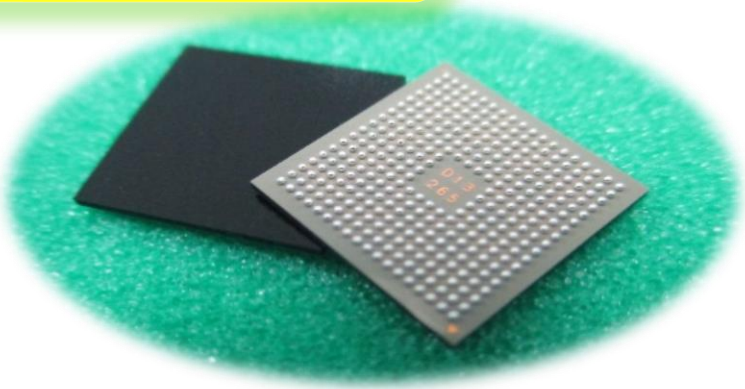
AOI GROUP
ONE STOP SOLUTION!

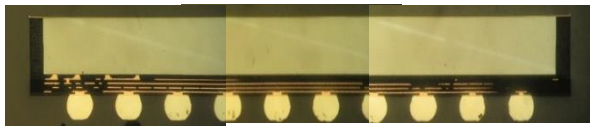
Drop Ship

FOLP® *for High Frequency application*

FOLP® Elemental technology （1）

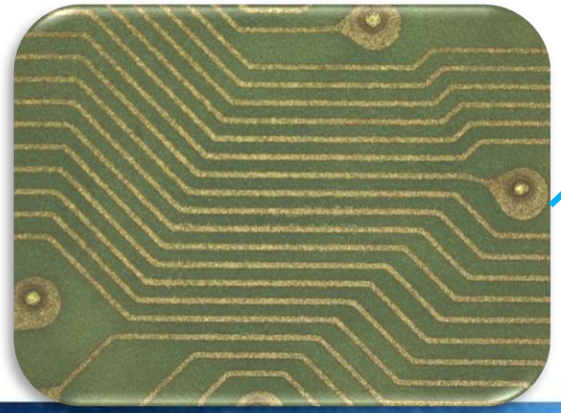
RF controller





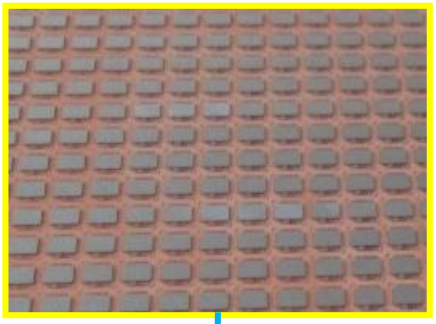
Fine Pitch RDL (Line=10μm)

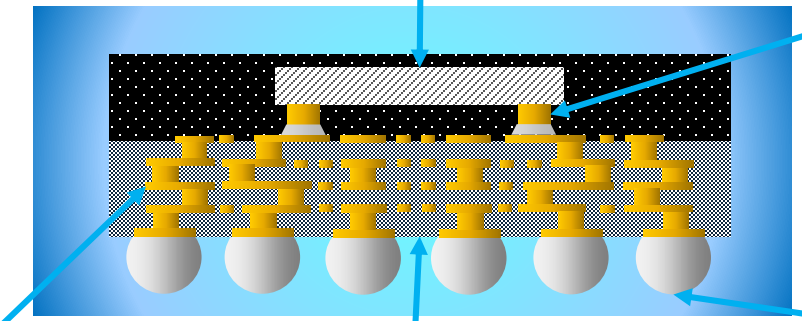
(Max 5 Layers in MP, 8 Layers in trial)



FC-Bonding

Si,SiGe,GaN,GaAs,Others(100μmt)





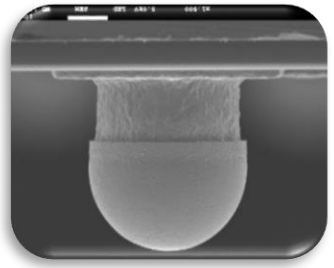
Low stress insulator

CTE (25～150℃)14ppm

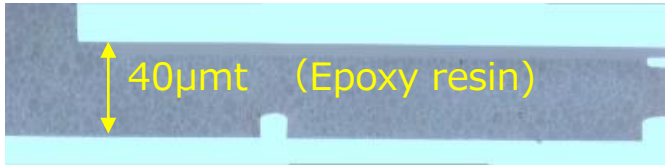
Young's modulus 10GPa

Cu Pillar Bump

40μm ～ Pitch

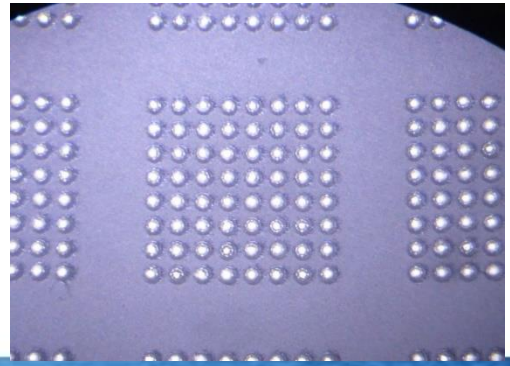


C2 bonding & encapsulation



Solder Bump

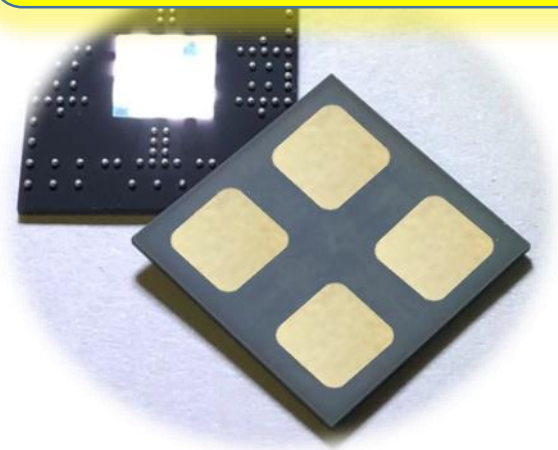
SAC, SACN,SACNBi Others



FOLP® Elemental technology （2）

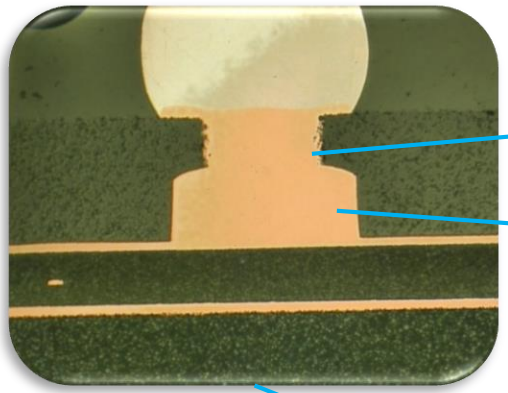
Applied Model

AiP Case



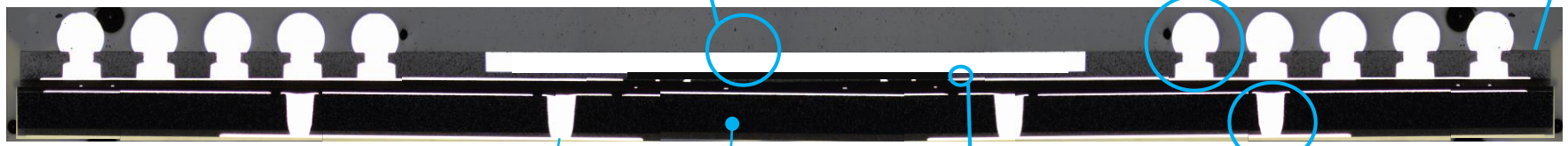
Backside Grinding

ToM(Terminal on Mold)



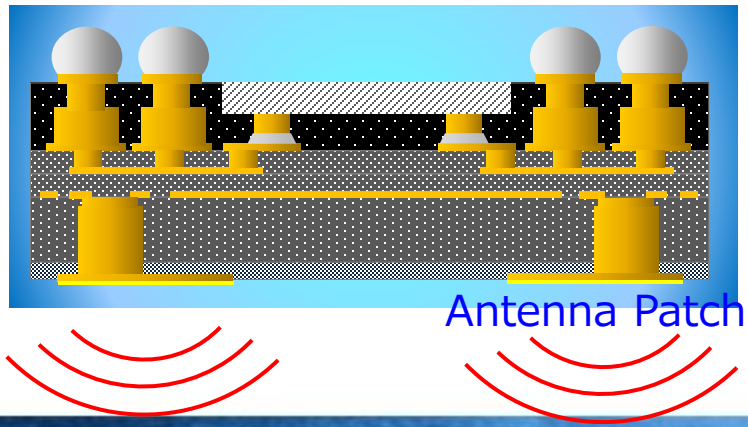
TRV(Through Resin Via)
+
Cu Post

Resin

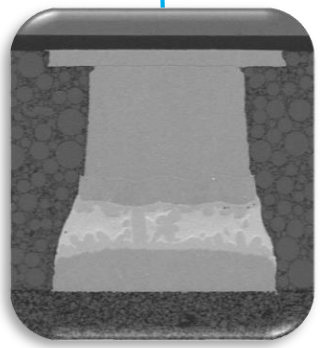


Accurate Via
alignment
on antenna

Low Df Isolation
(0.002 ~)



Antenna Patch



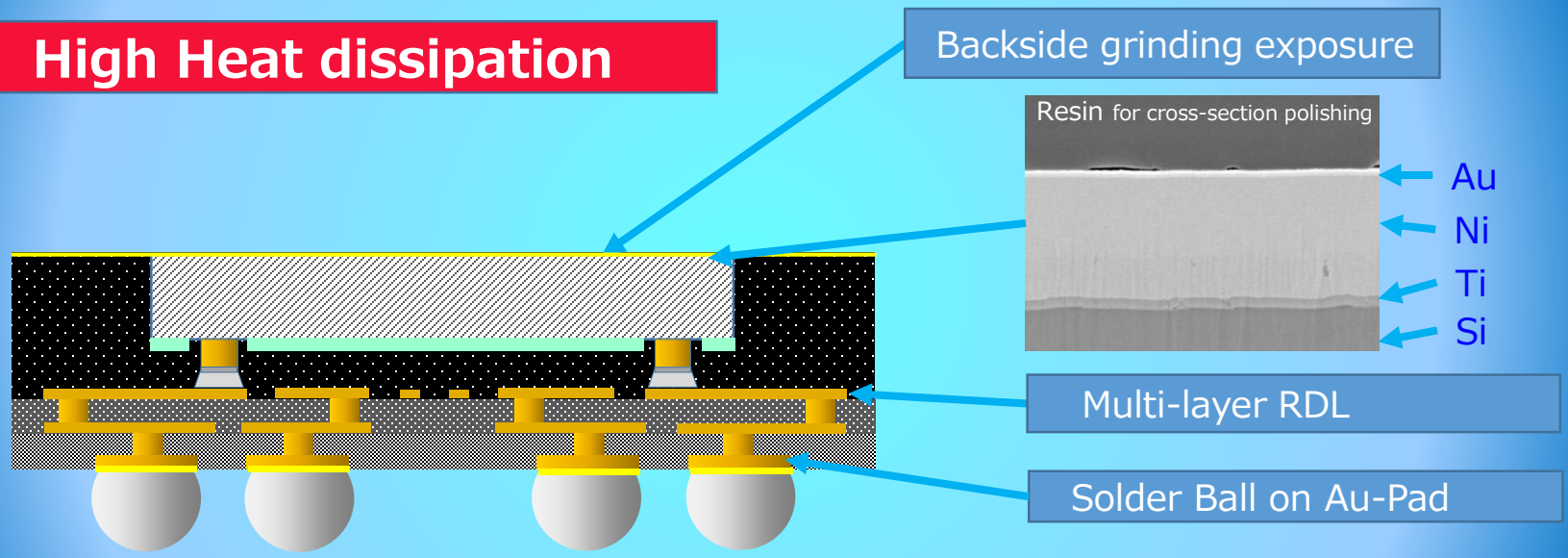
C2 bonding

200~400μm

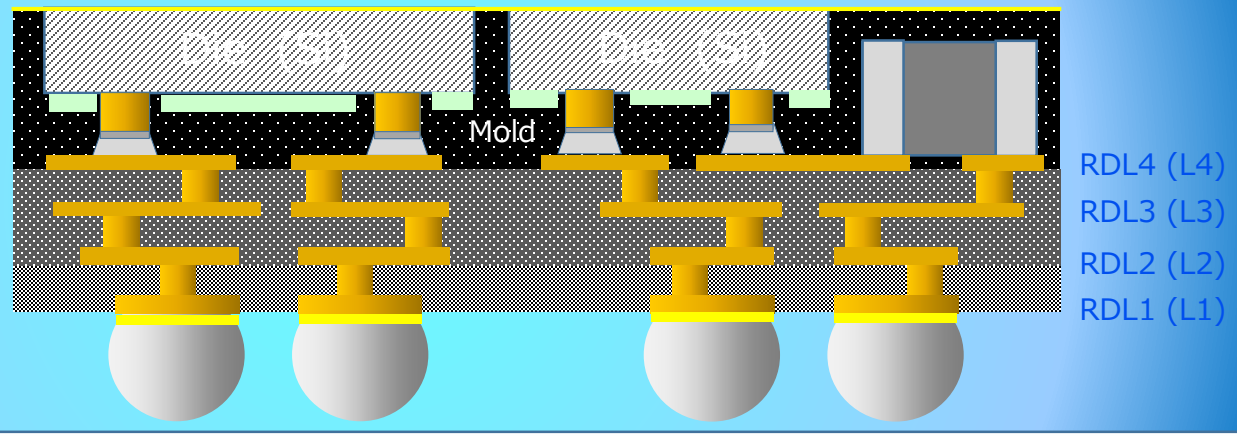
PLUG(Plugged Via)

Active＋Passive device FOLP® Module

High Heat dissipation



Thinner Module



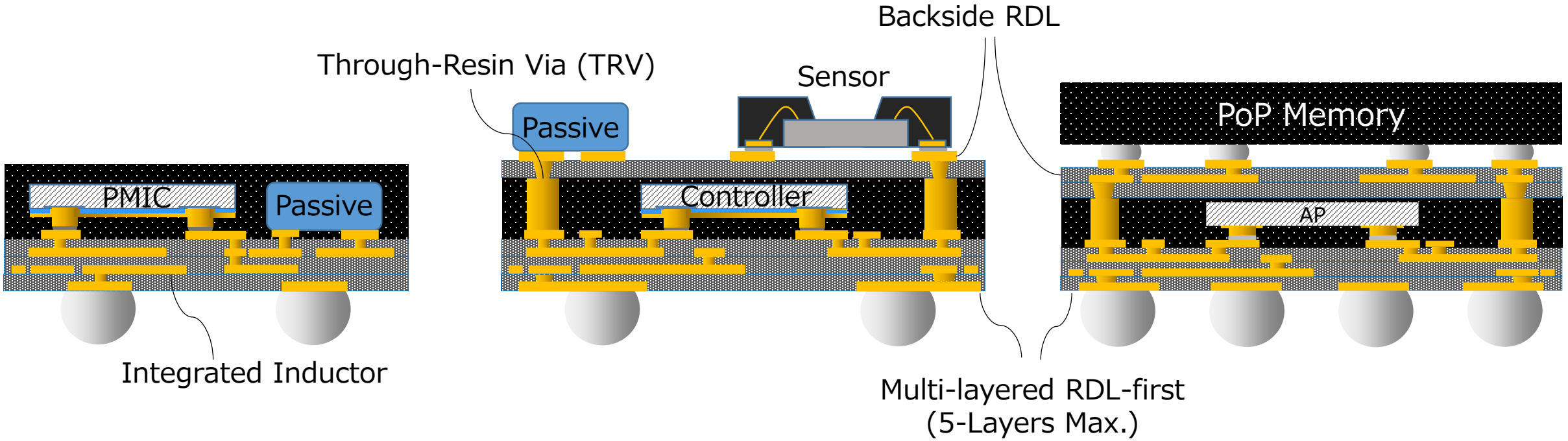
Flexible Structural Design for Various Applications

Epoxy-based RDL-first process enables flexible structural design for various applications.

Power Management

Sensor Module

Mobile Processor



FOLP® Process Advantage

1.High Yield : KG-RDL + KGD Combination

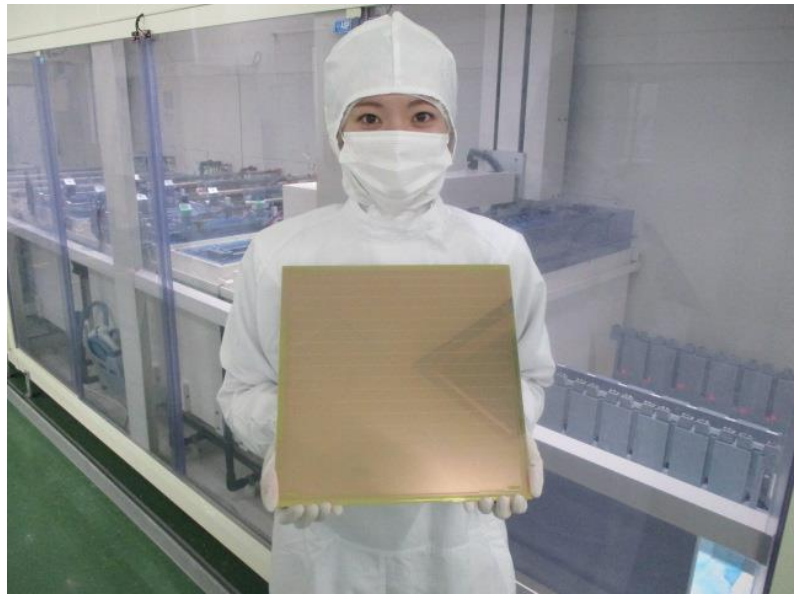
2.Short cycle time : Horizontal specialization Process
Wafer Bumping & Substrate (RDL) Process
+Assembly + Test Process

3.Cost effective : Mechanical de-bonding system
MUF(mold under fill) Process
300mm Sq. Panel

4.One stop solution in AOI electronics Group.

5.High Reliability : Modified Epoxy Resin (High Tg, Low Warpage)
Solder materials of various composition

6.High Performance : Good design flexibility
Low Dk,Df substrate materials for RF devices(5G⇒6G)
High heat dissipation, Low impedance for power IC



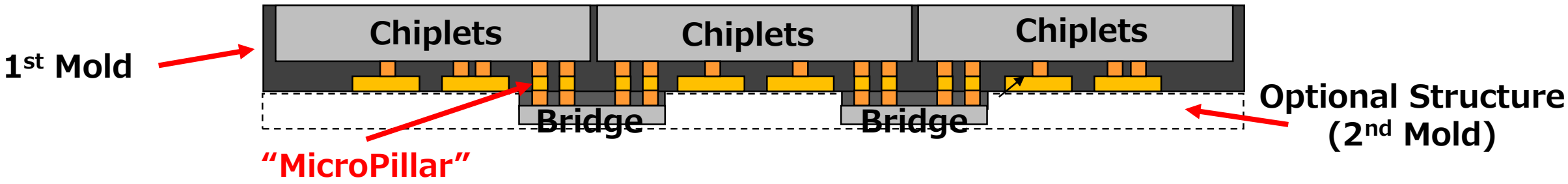
FOLP® *for Logic application (Chiplet integration)*

Conventional Chiplet Integration using “Interposer”

Technology	Si interposer	RDL interposer	Embedded Bridge interposer
Pros	✓ Technology maturity	✓ Excellent electrical characteristics ✓ Relatively low cost	✓ Excellent electrical characteristics ✓ L/S selectability
Cons	✓ Electrical characteristics ✓ High cost ✓ Size limitation (Wafer only)	✓ Feasibility of fine L/S at panel-level ✓ Need bridge assist in case of sub-micron L/S	✓ Complicated process and structure ✓ High cost ✓ Limited connection Pitch between bridge and chiplets

“Pillar Suspended Bridge”

AOI proposal



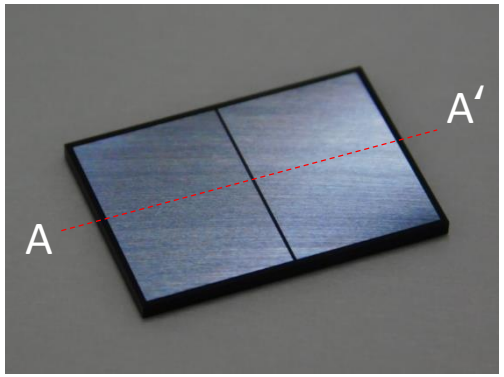
- **High positioning accuracy of bridges**
  - ✓ Face-Down bonder (~ 1 um)
  - ✓ Die shift is avoided by fixing with Micro Pillars
  - ✓ Not affected by variations in chip thickness
- **Simple process & material handling scheme**

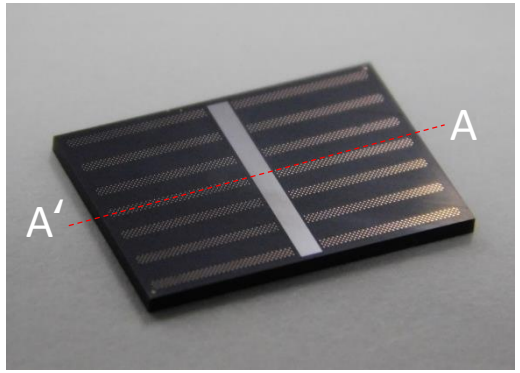
Excellent scalability

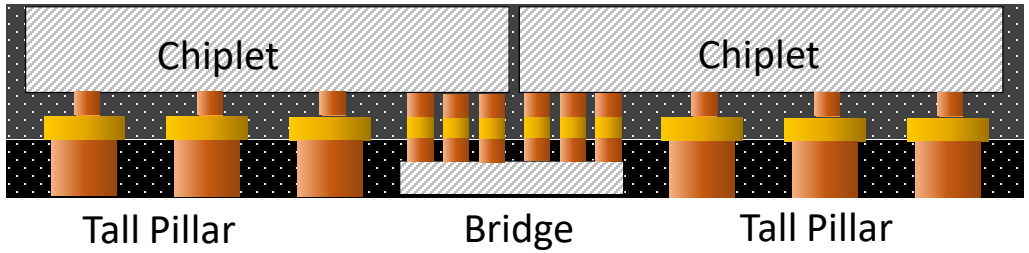
- ✓ ***Expandability to panel-level processing***
- ✓ ***Finer connection pitch for bridge*** *(< 20 um)*

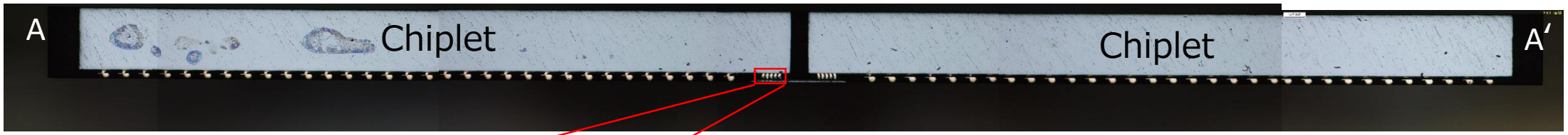
Internal Structure of Proof-of-Concept Sample

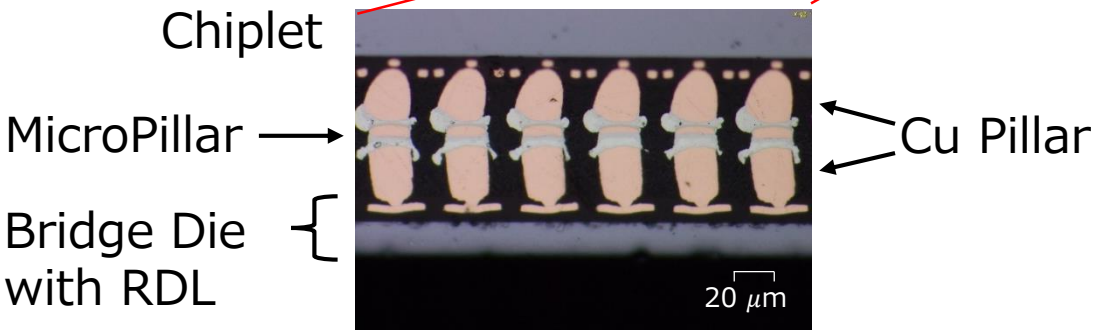
Die-to-Die interconnect by 20 μm thick Bridge











- MES2022 “A Simple Die-to-Die Bridge Architecture “ Evaluation with the Best Paper Award
- IMAPS 2022 “Chiplet Integration by Die-to-Die Pillar-Suspended Bridge”
- ECTC 2023 “A Novel Chiplet Integration Architecture Employing Pillar-Suspended Bridge with Polymer Fine-Via Interconnect”

FOLP® *for Power Module application*

Background

■ Applications：Power Supply System

Source：NTT Corporation

Source：TOYOTA corporation

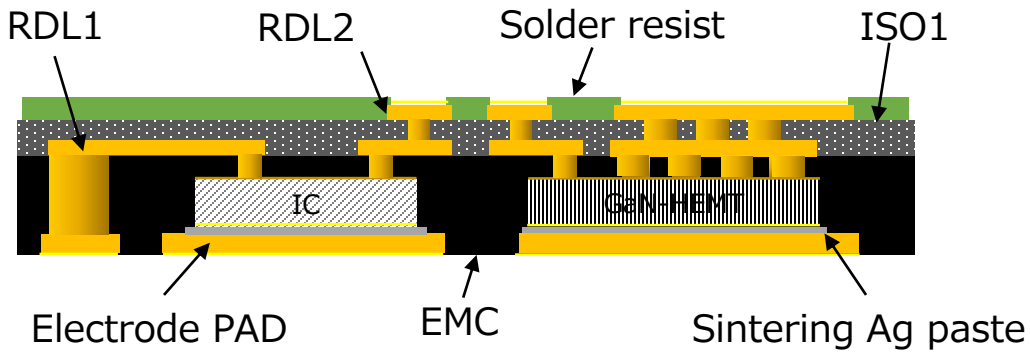
- ✓ Data centers and various power supply equipment shift from 12V to 48V systems.
- ✓ As power supply output current increasing, wiring resistance is a big issue about power distribution loss.
- ✓ Placing the power supply near the processor (CPU/GPU) will be an important for power integrity.
- ✓ Chip-embedded packages (PoP/CoP/3D-SiP) can shrink size and increase current density.

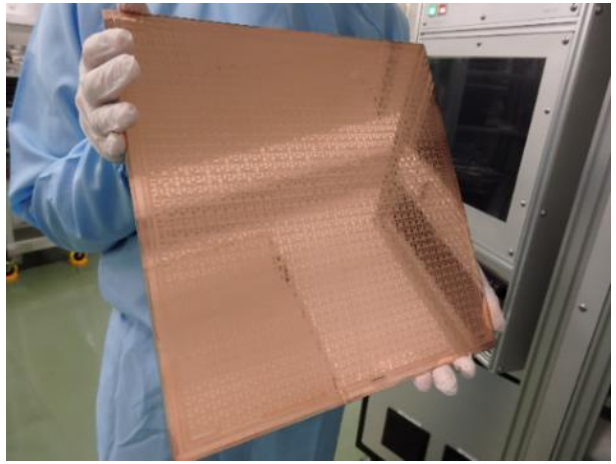
According to Texas Instruments 's white paper, they have brought an average module size reduction of 25 percent annually.

Source：U. Chaudhry et al, SiP Power Modules White Paper “Powerful solutions come in small packages”, Texas Instruments, page2

Introduction of Our Coreless Chip Embedded Technology

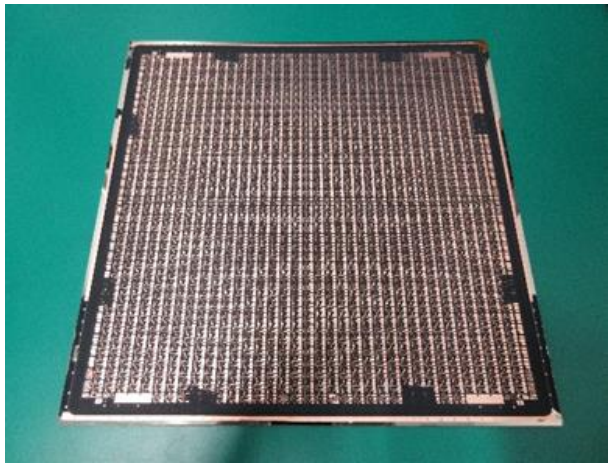
AOI's new approach of ***Ultra thinner, Higher heat dissipation***
chip embedded technology in analog and power solutions.





Features of this concept

- Unique Coreless structure
  - ①All Cu plating
  - ②Chip embedded method
  - ③Power customized fan-out processes
- Excellent thermal property
- SoC-like extra thin packages



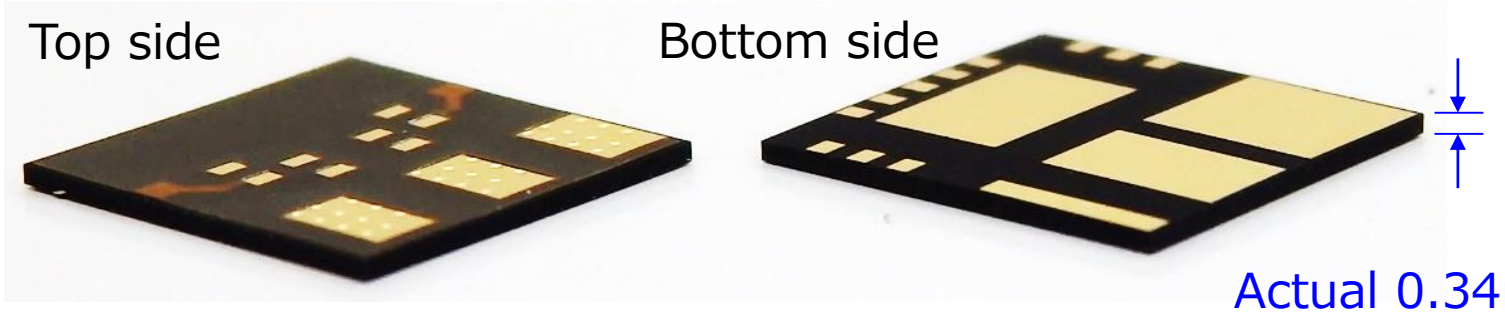
Trial production and evaluations for a Prototype

■ Prototyped package

New Coreless chip embedded module package

Top side

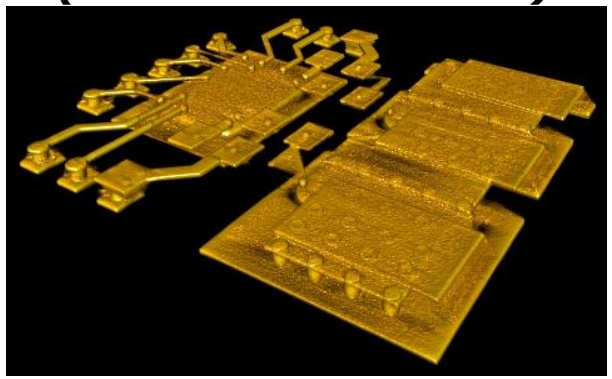
Bottom side



Actual 0.34mm

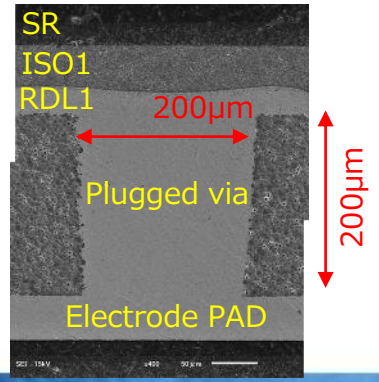
Package size : 7.0×7.5mm

X-ray CT 3D image (Internal structure)

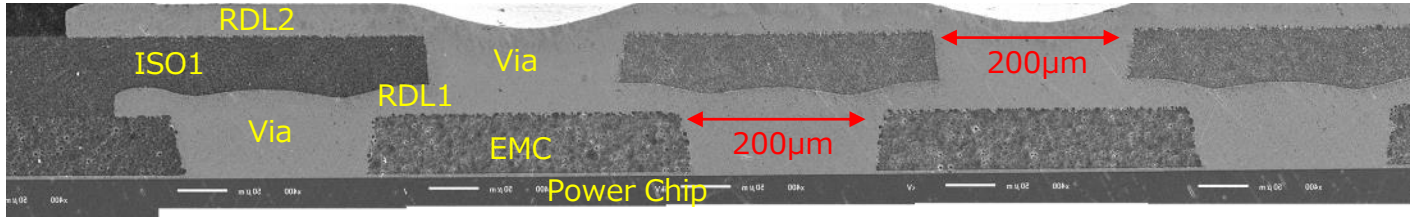


Actual Cross section

Cu plugged via

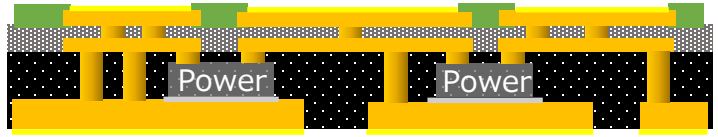
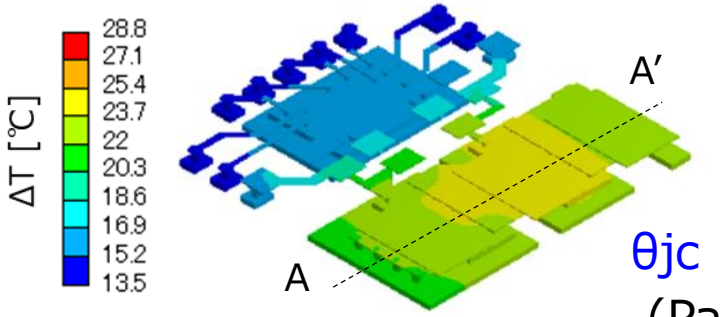
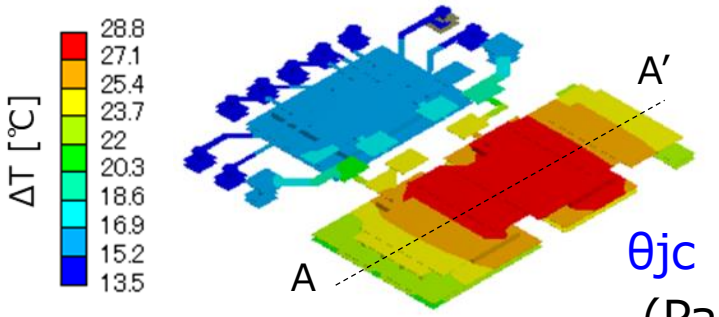


Direct Cu plating connection of power chips



Thermal Resistance Simulation with Our Concept Package

■ Simulation result

	Our Concept package	Prepreg package (assumption)
Structure	 t50μm	 t12μm t100μm t12μm Via : φ0.1mm, pitch 0.6mm
Thermal simulation result	Inside the Package image  θjc : 0.5 [℃/W] (Package only) Cross-section A - A′ 	Inside the Package image  θjc : 3.7 [℃/W] (Package only) Cross-section A - A′ 

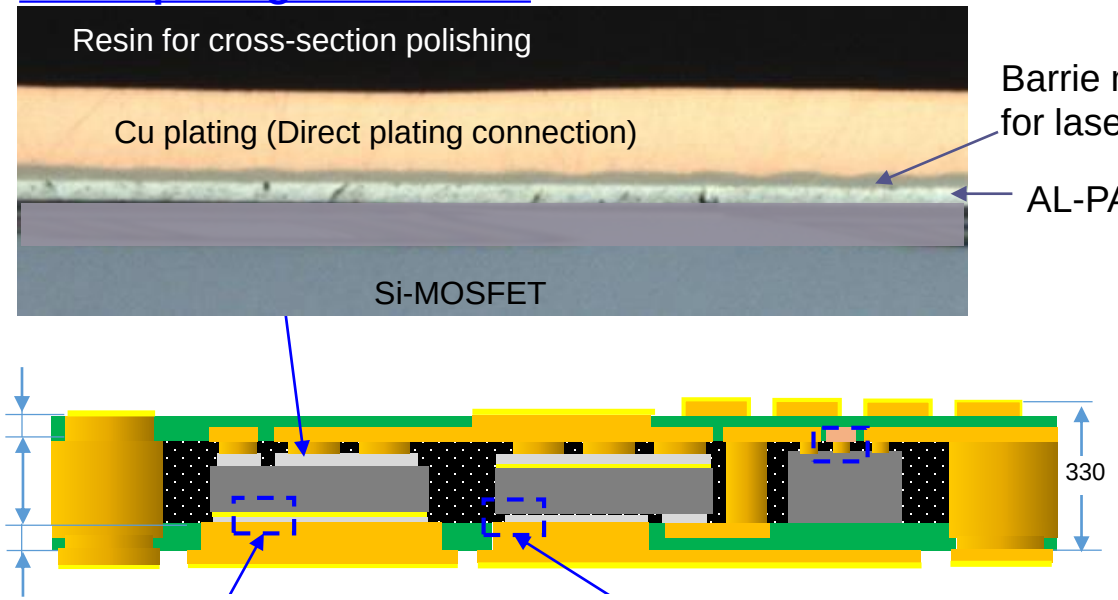
Embedded Multi-Chip in Molded Package

Package structure for Half-Bridge DC/DC converter

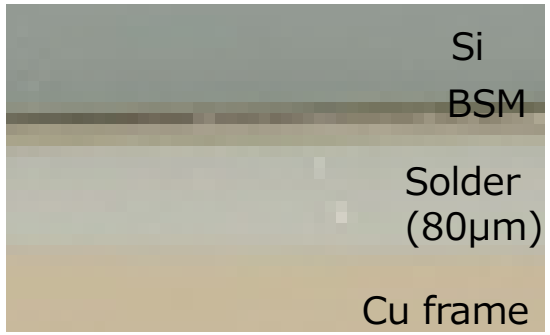
Solderless connect

⇒ ・Lower impedance
・Lower noise response
to high freq. switching

Direct plating connection

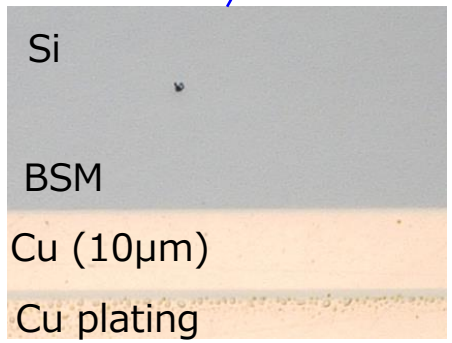


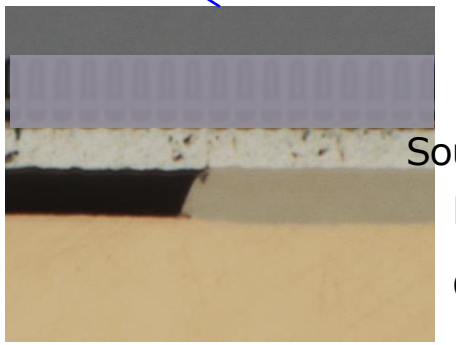
Solder connection



DB material
Electrical conductivity 50times
Thermal conductivity 38times

Direct plating connection





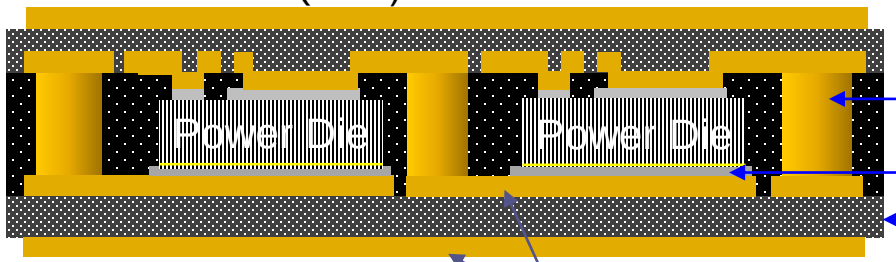
Embedded Multi-Chip in Molded Package

Under Development

Package structure for Inverter IC module

Embedded power package without DBC substrate

Cross-section (A-A')



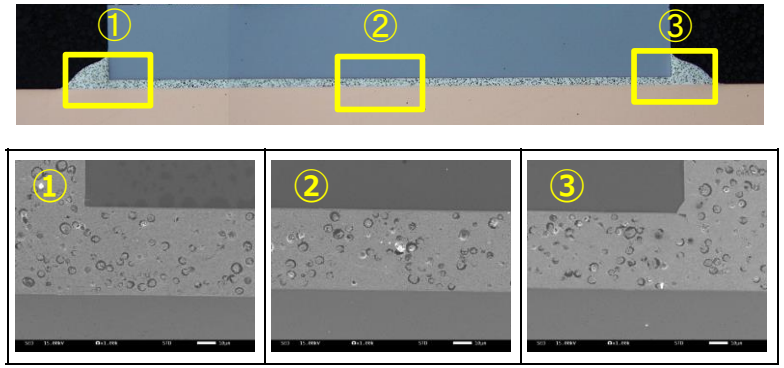
Large via

Ag sintered paste

Insulation layer
(Epoxy resin based material)

Dielectric voltage >4.0kV

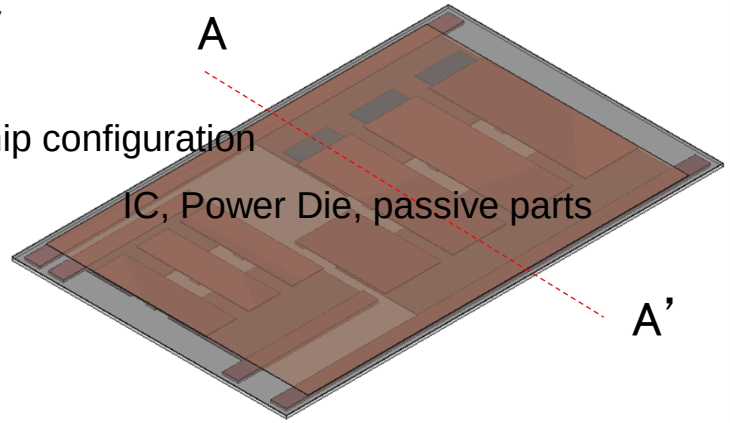
Cu metallization(plating)



Power die Ag sintered paste

Target ; Si, SiC etc.

3D-MODEL



Chip configuration

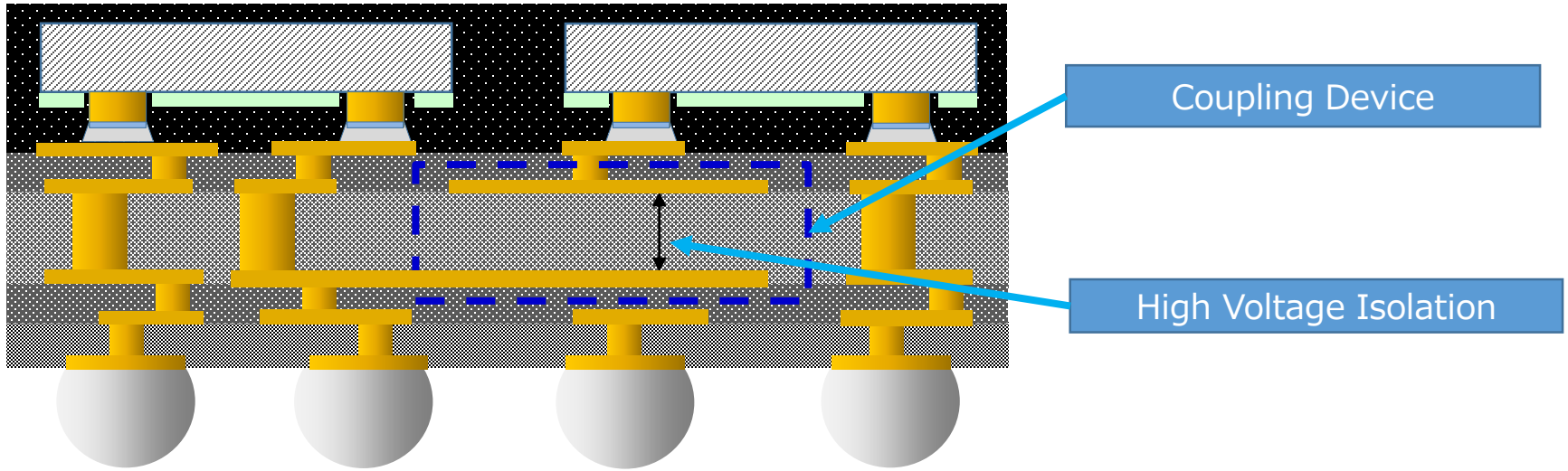
IC, Power Die, passive parts

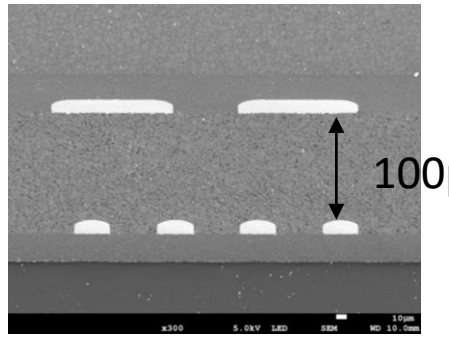
Prototype module

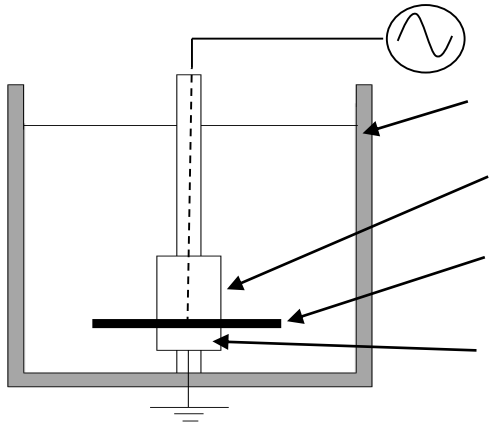
High voltage isolation by FOLP®

Embedded Coupling Devices

RDL High Voltage Isolation
for Digital Isolator , Isolation Power supply etc.







Oil bath (Silicon oil)
Upper electrode
Sample
Under electrode

Based on ASTM-D149

Isolation(µm)	kV/mm
100	122.7

ATTENTION

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