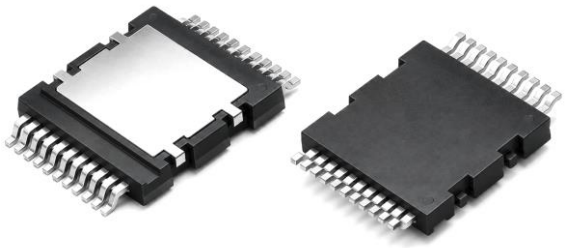
開発中

Q-DPAK
(JEDEC MO-354)



次世代パワー半導体の性能を、パッケージで変える。

TOP-SIDE COOLING
ヒートシンクに直接放熱可能な上面放熱構造で、
高い熱性能を実現。

LOW INDUCTANCE
最適化された構造により、寄生インダクタンスを
最小化し、高速スイッチングに貢献。

KELVIN SOURCE
ケルビン接続により、ソース端子の寄生インダクタンス
を低減し、安定したスイッチングと低損失を実現。

APPLICATIONS

AI DATA CENTER

UPS / ESS / Server Power

xEV

Charger / Inverter / OBC / DC-DC

RENEWABLE ENERGY

Solar Power Inverter

国内一貫生産
設計・開発から製造まで、
すべての工程を国内で完結。

Built for GaN & SiC.
Al Wire / Cu Clip • Assembly → Test

Q-DPAK ホワイトペーパー
背景、市場・技術動向、製品詳細などを掲載

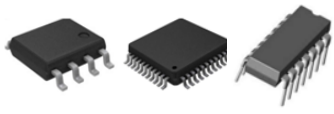
https://tech.aoi-electronics.co.jp/technology/

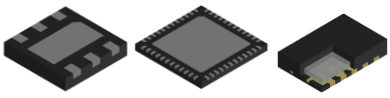
AOI ELECTRONICS CO.,LTD.

AOI Group Packaging Service

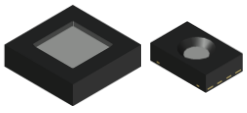
Package Line-Up

SOP/QFP/DIP | DFN/QFN | Sensor | WL-CSP | LGA

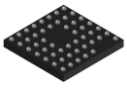


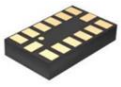


Flip Chip



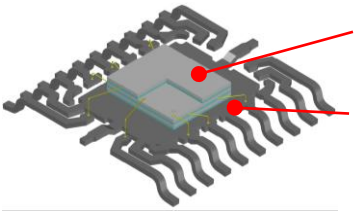
Open Cavity





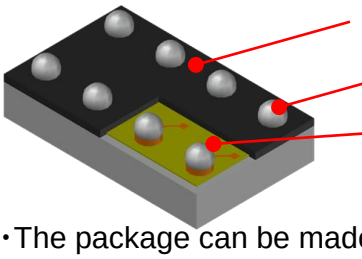
Element Technology

Film on Wire



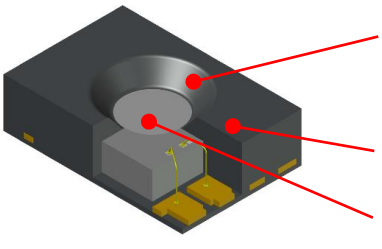
- Wire on bonding PAD embedded with DAF
- Same size chip stack is possible
- Footprint miniaturization is possible

WL-CSP



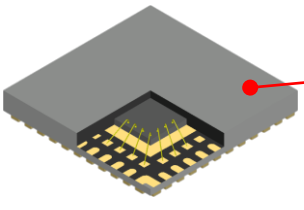
- The package can be made smaller and lighter.
- Shorter traces reduce resistance.
- Protection of circuit surfaces and sides using resin

Open Cavity Molding



- Chip surface can be exposed
- Chip on open cavity is possible
- Open cavity shape can be customized

Electromagnetic Shielding



- The shielding material uses sputtering technology
- Standard material is Ni+Cr
- The shield is processed on all four sides except the terminal side.

Package Line Up for QFN / Flip Chip QFN / Open Cavity

	Variations by package thickness												Option	
	016	025	03	04	05	06	07	08	09	100	110	160	Wettable Frank	Shield
DFN / QFN	○	○	○	○	○	○		○	○			○	○	
Flip Chip QFN			○	○	○	○		○	○			○	○	
Open Cavity PKG						○	○	○		○	○		○	
LGA						○		○						○

■Available the number of pins : 4pin～56pin ※Larger pin number and larger size：Contact to sales.
■Available package size : 1010～7070 ■Flip Chip type LGA : Contact to sales.

AOI ELECTRONICS CO.,LTD.

DPCC™
（Direct Printed Copper on Ceramics base substrate）

What is DPCC™

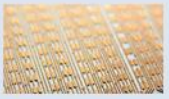
POINT

Forming with Copper Paste
- ✓ Thick Copper Patterns
- ✓ Narrow Spacing

・**H**igh current and high heat dissipation substrate applications
・**L**ogic circuits can also be formed on the same substrate as heat dissipation circuits
・**A**vailable thick copper with narrow L/S

1 **Over 1,000μm* Circuit Thickness**
Circuit pattern thickness suitable for power semiconductor substrates can be selected.

2 **Min.25μm* Pattern Spacing**
Enables high-density wiring formation that exceeds conventional DBC/AMB substrate.



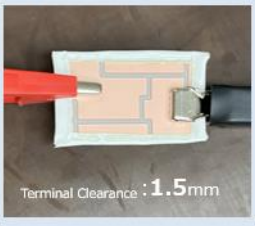
3 **Various Ceramics Substrate**
Available Cu Circuit patterns on various ceramic substrates.
(Ex. AL_2O_3 , ALN , SiN etc.)

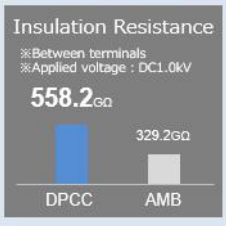
*Depends on printing conditions

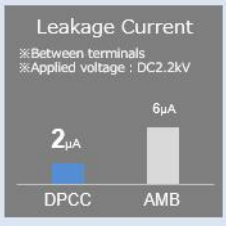
Product Features

High Insulation Resistance

・Eliminating the etching process improves insulation between terminals.
・High insulation resistance can be obtained with a narrower space.

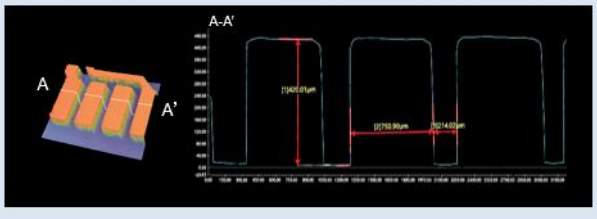






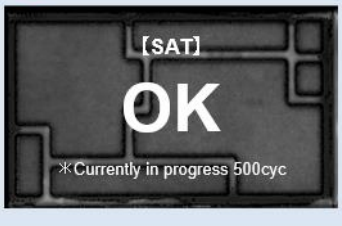
Thick with Narrow Spacing

・Print method : Possible to form L/S that is difficult to achieve with etching.
・High aspect ratio terminal formation.



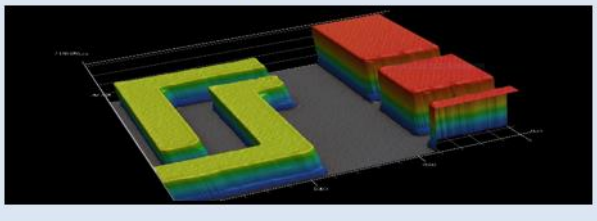
Reliability Test Results

・Temperature Cycle Test :-40℃(30min)⇔125℃(30min)
・Currently under continuous evaluation (～2000 cyc)

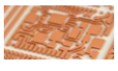
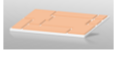
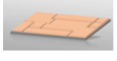
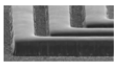


Various Shapes

・Possible to form circuit with different thicknesses.
・Possible to add protrusion shapes.



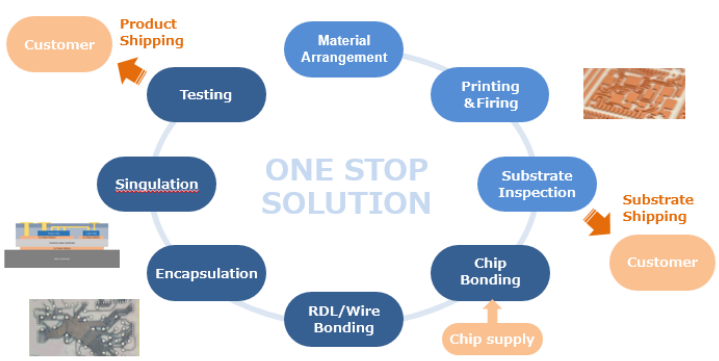
Design Rules

	DPCC™	DBC	AMB	MSAP
Base material	AL^2O^3, ALN, SiN etc.	AL^2O^3	ALN, SiN	AL^2O^3, ALN, SiN etc.
Patterning material	Cu	Cu	Cu	Cu,Ag,Au,etc.
Max. size	No limit	Depends on Cu foil size/Substrate size	Depends on Cu foil size/Substrate size	Depends on Substrate size
Max. thickness	＞1,000μm*	<800μm	<800μm	<50μm＊
Min. L/S	＞25μm*	Pattern thickness	Pattern thickness	＞10μm＊
L/S tolerance	±50μm	±50μm	±50μm	±10μm
Surface plating	Available	Not available	Not available	Available
Process	Just a printing process (Suitable of mass production)	Complicate	Complicate	Plating and etching etc.
Thermal conductivity	109 W/(m･K)	N.A.	113 W/(m･K)	N.A.

*Depends on design

One Stop Solution

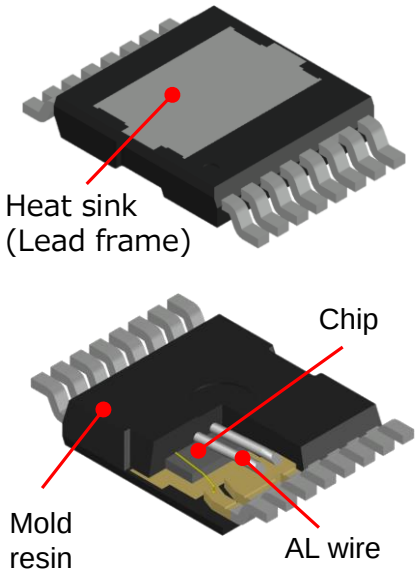


Available from substrate manufacturing to product assembly.

AOI ELECTRONICS CO.,LTD.

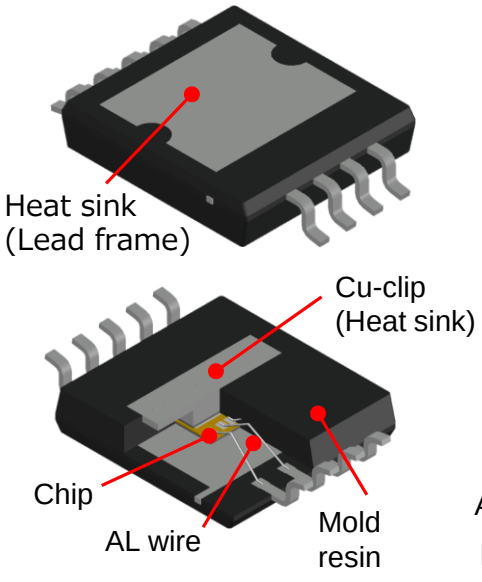
Package specialized for power

Top or Bottom Heat Dissipating Package



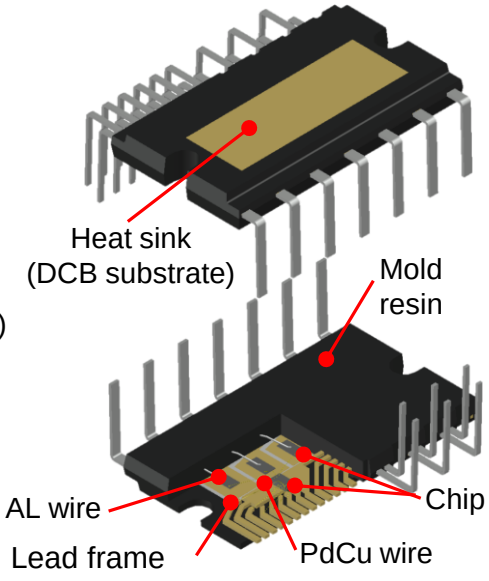
・Al-Wire is standard, but Cu clip is also available.
・By selectively changing the lead forming, it is possible to choose between surface heat dissipation and backside heat dissipation.

Double-Side Heat Dissipating Package



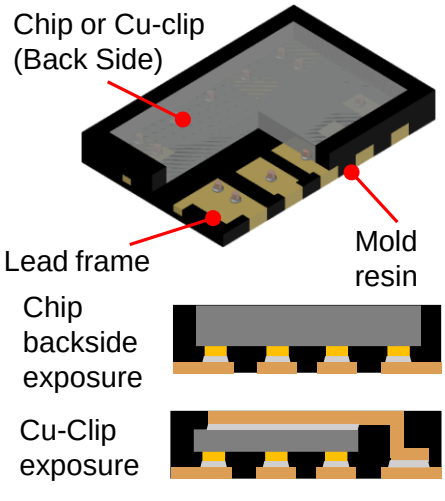
・Improved heat dissipation by using an dual gauge copper strip lead frame.
・Exposed area can be selected arbitrarily.
・High-precision parallel mounting exposes heat sinks on both sides(no polishing).

High Heat Dissipating Package using Insulated Substrates



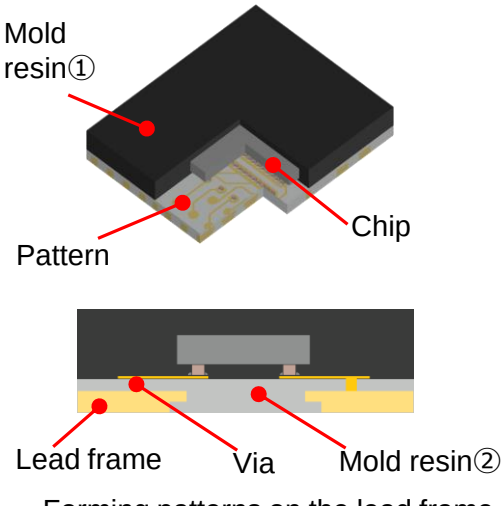
・Modularization of 2 IC chips and 6MOS chips in one package.
・An electrically insulating heat sink is used. DCB substrate is standard, but AMB substrate with better heat dissipation properties is also available(Our original DPCC substrate can also be mounted).

Exposed chip(Cu-clip) backside structure Flip chip



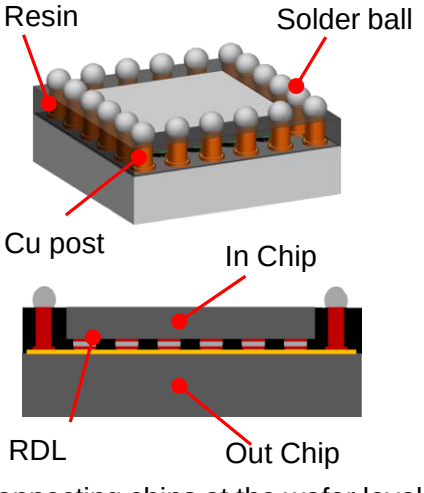
・Flip-chip structure exposes the backside of the chip for improved heat dissipation
・Exposed surface can be replaced with Cu-Clip.
・Using a flip chip makes it possible to reduce on-resistance

MIS structure (Molded Interconnect Substrate)



・Forming patterns on the lead frame using redistribution layer technology.
・ it is possible to form a mounting pattern that matches the pad layout of the chip
・In the case of single-layer, it is possible to make it via-less and reduce the thickness.

Chip on Wafer Structure



・Connecting chips at the wafer level allows for miniaturization.
・Mounting at wafer level reduces parasitic capacitance and increases speed.
・It is possible to mount chips with different processes on the same wafer.

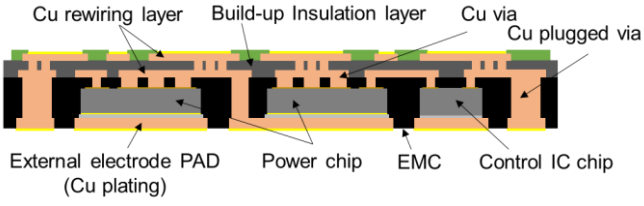
AOI ELECTRONICS CO.,LTD.

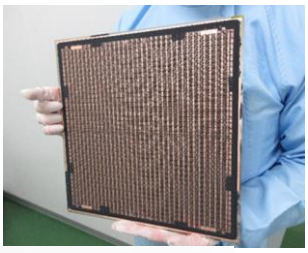
Advanced Power Panel-level Package Technology

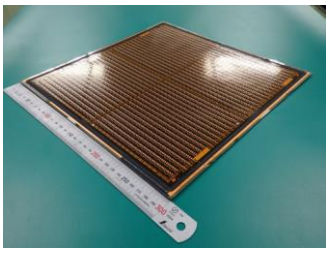
DC-DC half-bridge application (GaN HEMT module)

Focusing on power application using chip-embedded technology

- 300 mm square Panel Form
- Miniaturization and Thinner
- Higher current density
- Excellent double-sided cooling concept
- Robust all Cu plated interconnects

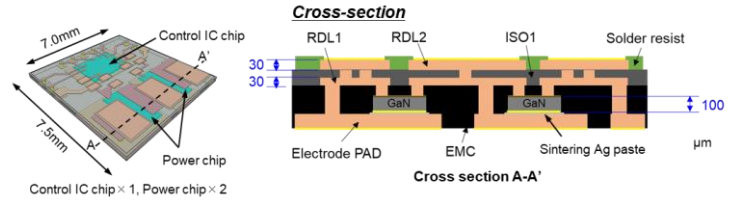


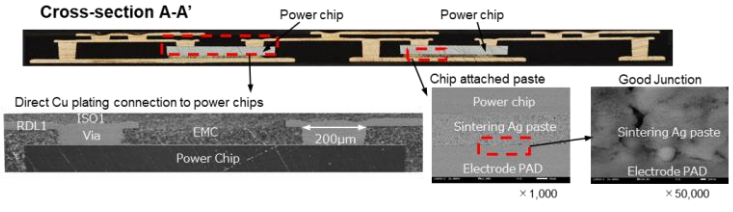




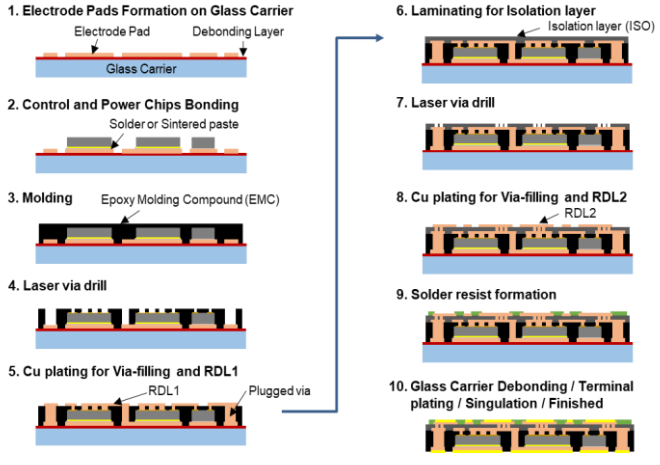
Prototype
Package size : 7.5 × 7.0mm
Thickness : 0.34mm

Trial production and evaluations for a Prototype





Process flow *From panel substrates to package assembly in-house*

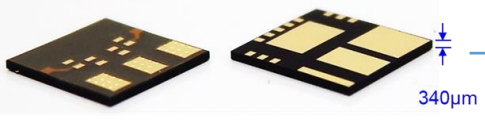


Chiplet integration device application

Suitable power delivery by IVR (Integrated Voltage Regulator)

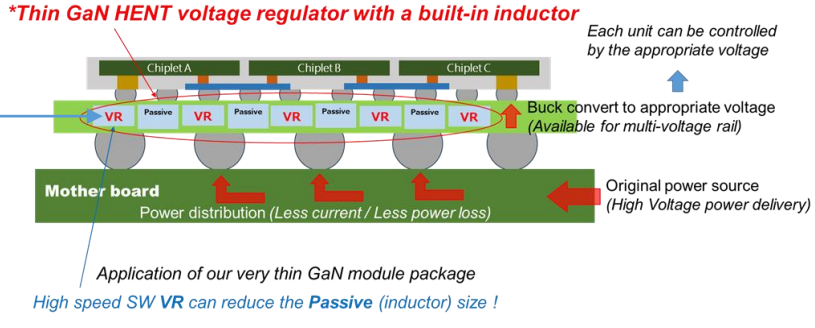
Target Application：Power Supply System for AI Data Center

New GaN HEMT power module

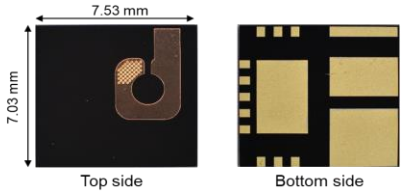


Package size : 7.0×7.5mm

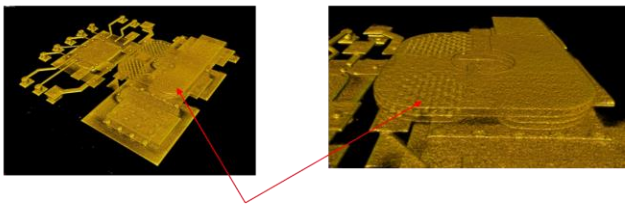
■ Suitable power delivery by IVR (**Integrated Voltage Regulator**)

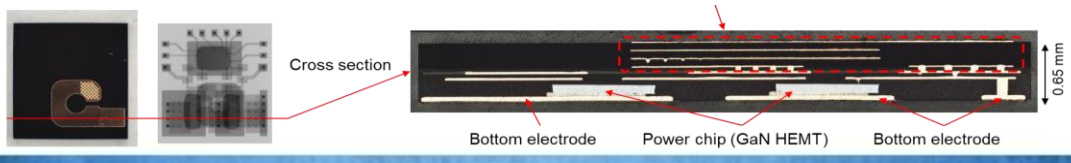


Prototype package outline



X-ray CT 3D image





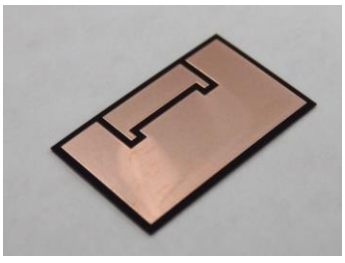
Advanced Power Panel-level Package Technology

Inverter application (SiC Sub assembly module)

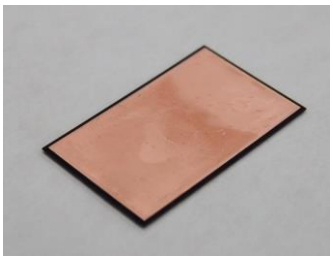
Target Application：Inverter for Vehicle

Prototype

Top

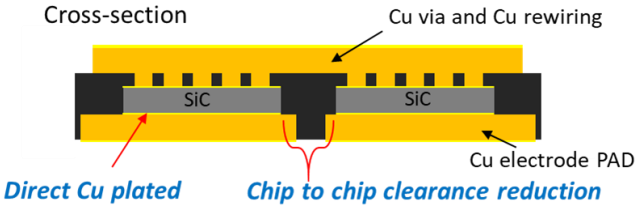


Bottom



Module size : 15×10mm

Direct double-sided Cu plating connection to SiC chip



SiC chip : 2 parallel

■TCT results for Direct Cu plated

Reliability test conditions（Component Level Reliability）

Test Items	Condition
Pre-Condition	The baking condition is 125 ℃ 24h. MSL = LEVEL1 Ta=85℃, RH=85%, storage=168h Reflow soldering heat stress (3times)
Thermal Cycle Test (TCT)	Ta= -65℃⇔150℃

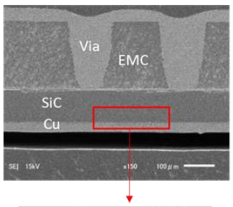
Reliability test results

TCT	n=22	Time	100 cycles	300 cycles	500 cycles	1,000 cycles
		Result (Failure rate)	0/3	0/3	0/3	0/3

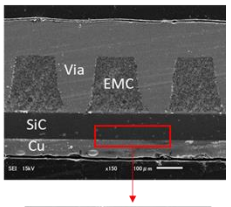
※Result :Cross-sectional SEM check by sampling

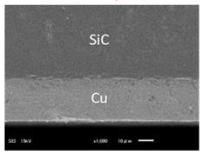
Cross-sectional SEM after each cycle

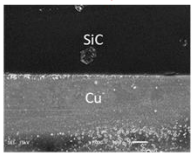
After 500cyc



After 1,000cyc



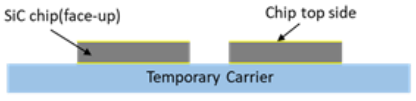




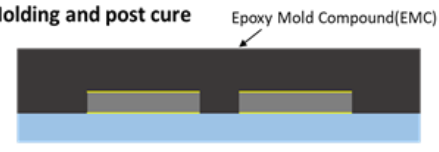
No delamination and cracking

Process flow

1. Chip bonding on temporary carrier



2. Molding and post cure



3. Temporary Carrier debonding

4. Electrode PAD formation with Cu plating