Introduction for **FOLP** ®Technology

FOLP *® （**F**an-**O**ut **L**eaded **P**ackage)/ FOPLP*

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Development background

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Technical Packaging trend for Applications

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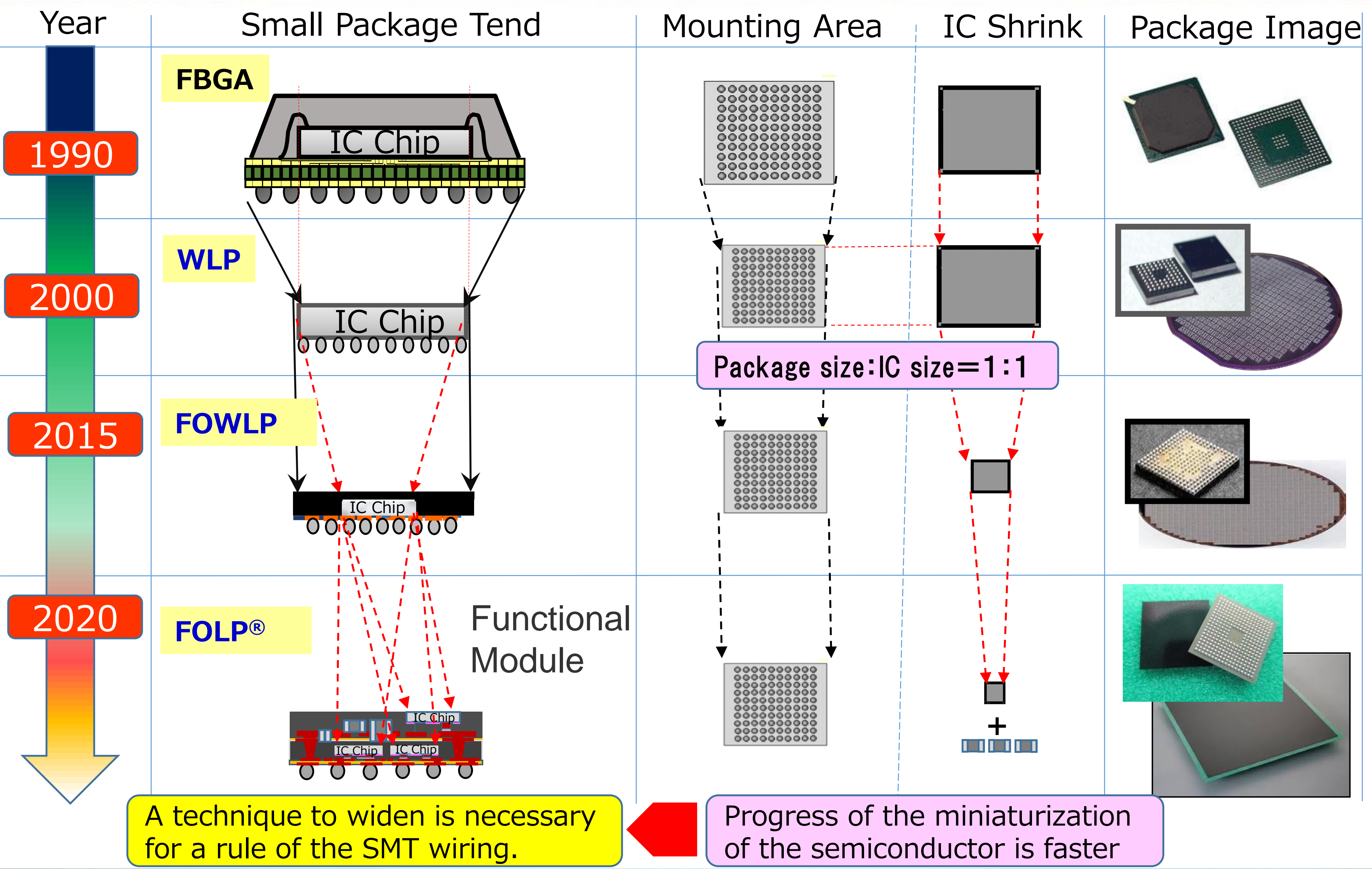
BGA Package miniaturization trend for mobile· IoT/5G



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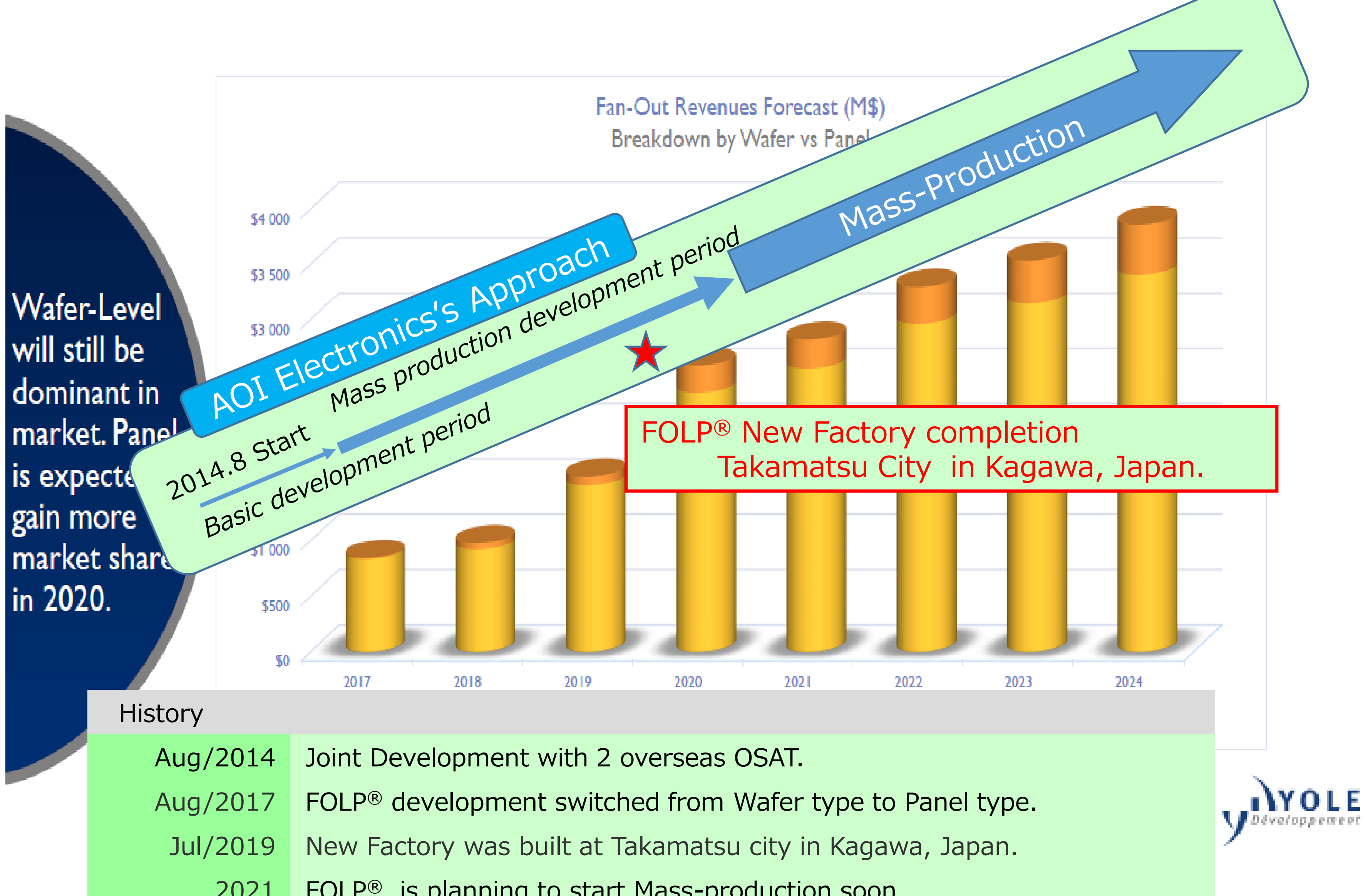
FOLP® Development History



History	
Aug/2014	Joint Development with 2 overseas OSAT.
Aug/2017	FOLP® development switched from Wafer type to Panel type.
Jul/2019	New Factory was built at Takamatsu city in Kagawa, Japan.
2021	FOLP® is planning to start Mass-production soon.

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AOI Target's application and specification

	Level 1	Level 2	Level 3
Application	RF , PMIC. MEMS , Sensor	BB Combo , Single-Chip High-end	APE , SiP
L/S Rule Target	(L/S:20/20-15/15)	(L/S:10/10um)	(Under L/S:5/5um)
Cu Pillar Pitch	80～200um	40～80um	Less than 40um
Example of Current PKG (Smart Phone)	RF: Front End module RF: Power amp module RF: Wi-Fi BT GPS module RF: Antenna SW module RF:RF Transceiver PMIC Electric Compass Accelerometer Gyroscope NFC	Baseband Processor APP PMIC	POP DRAM Logic DRAM Logic
Expect Specification of FOPLP	Size:2-6mm sq. 1chip:compass,P.M. 1Layer 2chip:Another 1-2Layer	Size:6-10mm sq. 1chip:P.M. , APP 1Layer 2chip:BBcombo 1-2Layer	Size:10-20mm sq. APP&DRAM 2chip side by side SIP 2Layer

1ST Target → Next Stage Target

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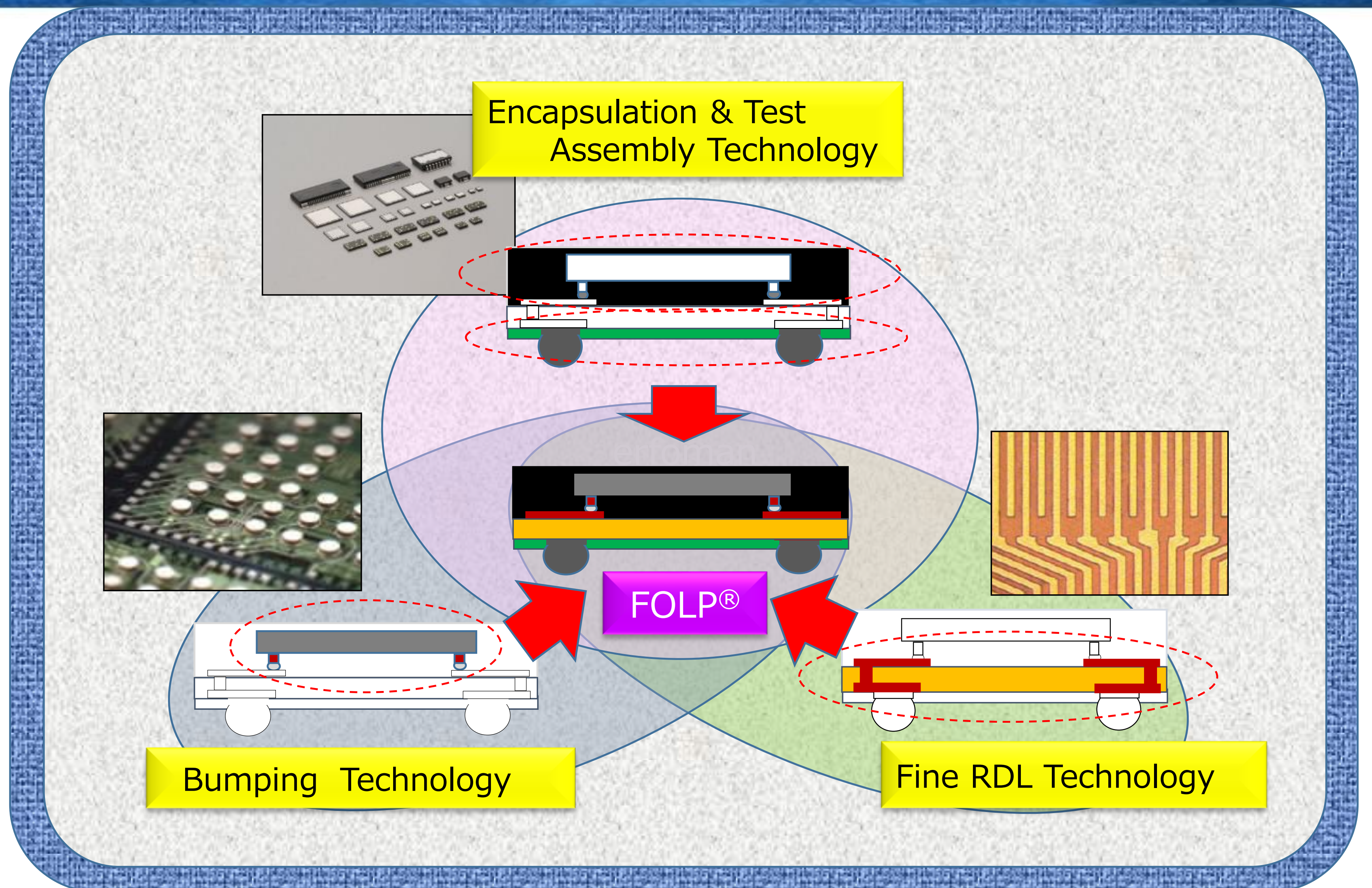
AOI Group Package Technology



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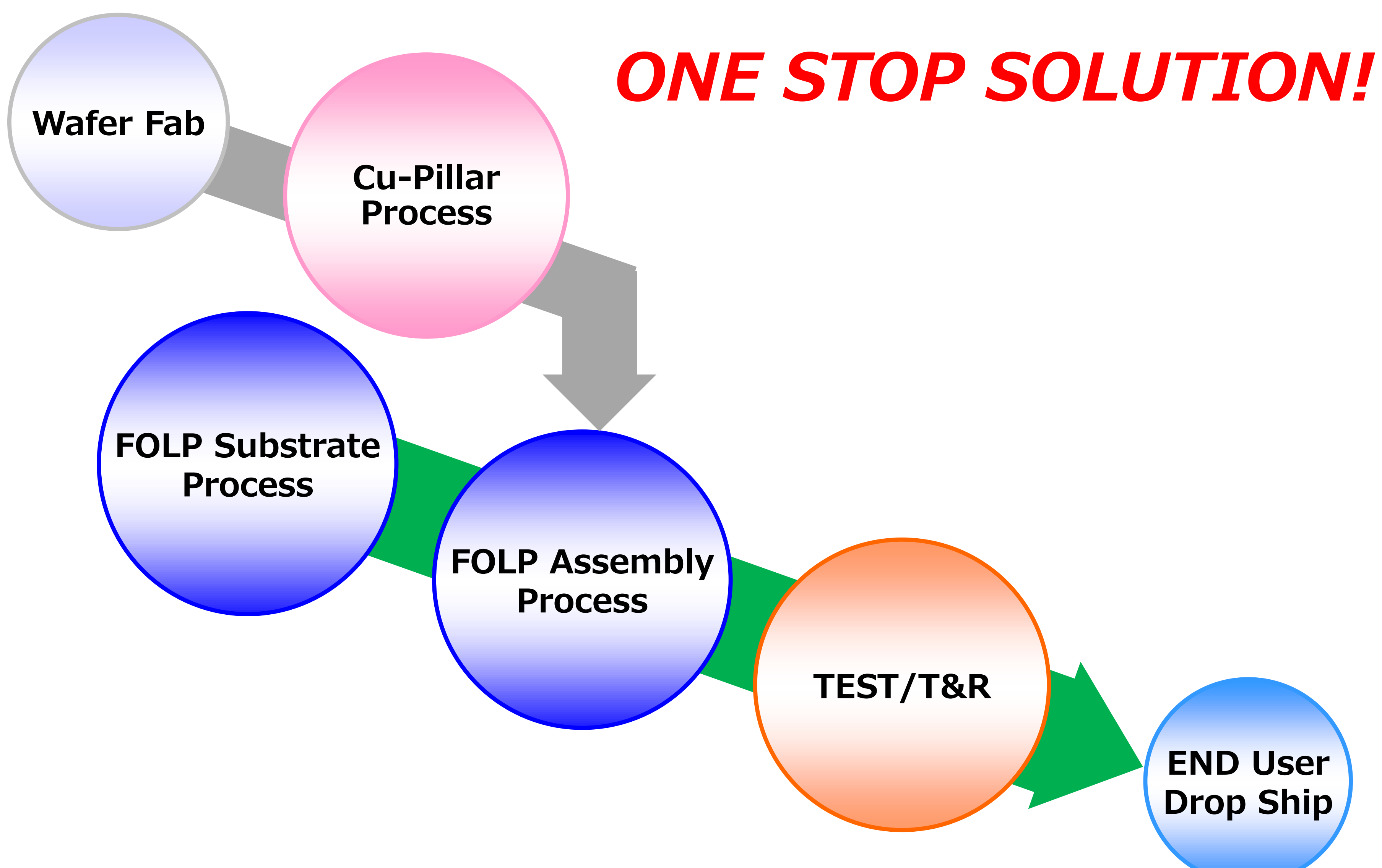
FOLP® Manufacturing Flow



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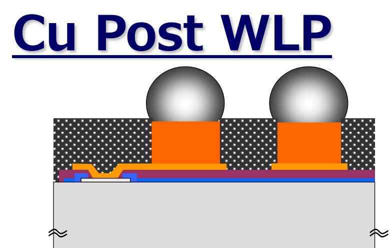
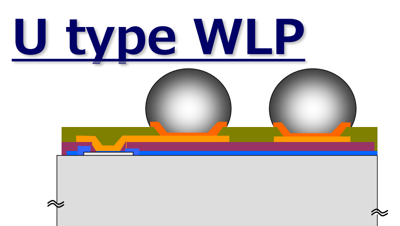
Types of WLP and Bumping new development

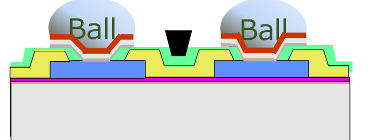
Cu Post WLP



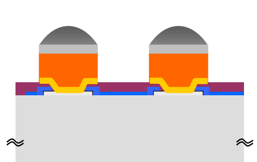
U type WLP



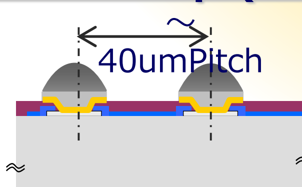
With Solder ball



Cu Pillar



Micro Bump (Solder)



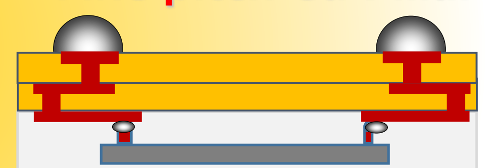
Developing new technology

- Improving WLP reliability
- Cu pillar technology
- FOLP® technology
- N in 1 Module technology

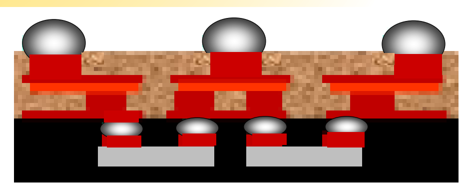
etc.

Improving WLP reliability

Fine pitch Cu Pillar



FOLP®(FOPLP/Chip Last)



N in 1 (FOLP® module)

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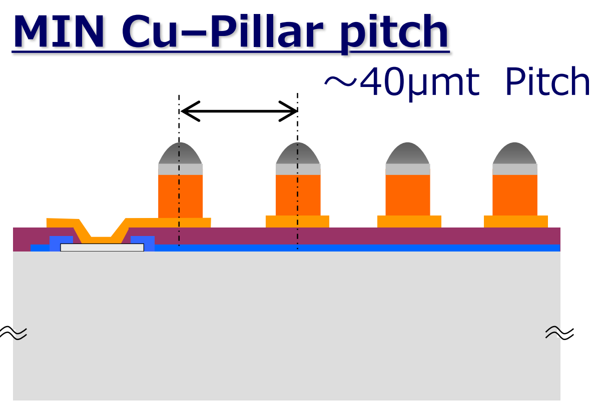
Cu-Pillar Variation

[μm]

	Current
Wafer Size	6,8&12 inch
Aspect	2.5
MIN Diameter	20
MAX Height	50
Terminal structure	SnAg/Ni/Cu SnAg/Cu

MIN Cu–Pillar pitch



Cu pillar on Al-Pad

RDL-Cu-pillar

Φ25× t40

Φ45 × t50

Φ70× t45

a

b

Aspect a : b ≒ 1 ： 1

AOI Electronics's Cu-pillar bumping are well-known for their reliability due to its long history of achievements from 2006y.

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FOLP® (FOWLP) Process Flow (RDL First Method)

FOLP Substrate Process

Cu-Pillar Process

FOLP Assembly Process

TEST/ Tape & Reel

・Support Plate

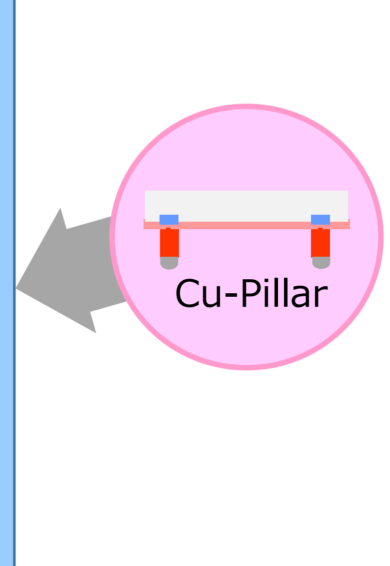
・RDL

・FC-Bonding

・Molding

・Solder Ball & Reflow

・Testing



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FOLP® Process Merit & AOI's Advantage

1.High Yield : KGD +KG Substrate Combination

2.Short cycle time : Horizontal specialization Process

*Wafer Bumping
*Substrate(RDL) Process
*Assembly +TEST/Tape & Reel Process

3.One stop solution in AOI-ELECTRONICS Group.

4.High reliability : -Modified Epoxy resin
-Solder materials of various composition attach

5.High performance :AOI can use the Low Dk,Df substrate materials
for RF 5G devices.

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Example of application for FOLP®

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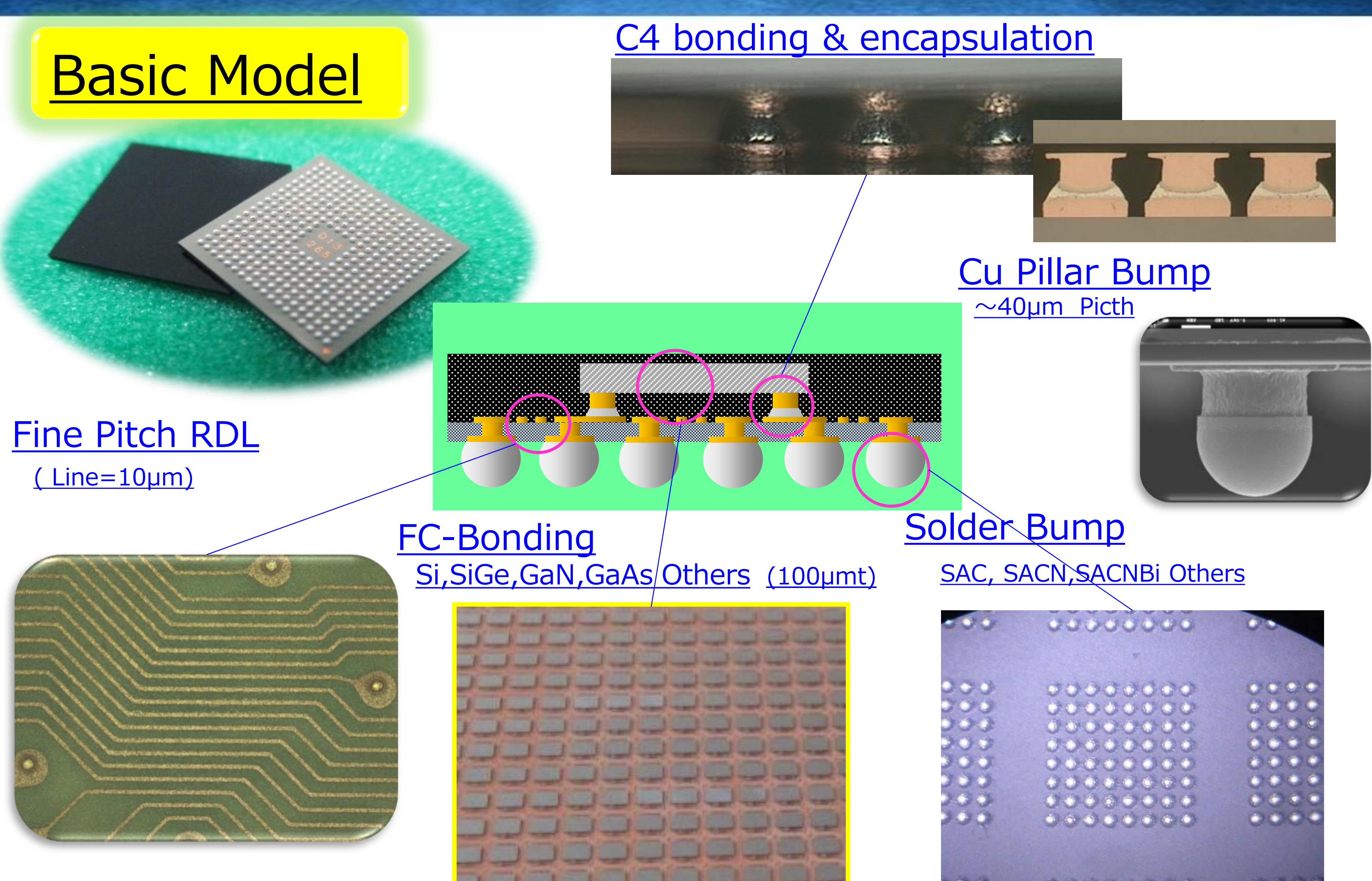
FOLP® Elemental Technology （1）



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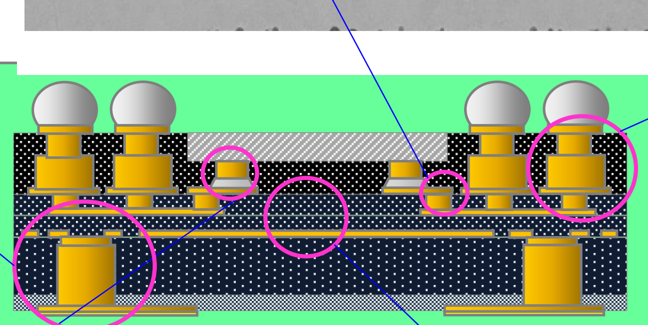
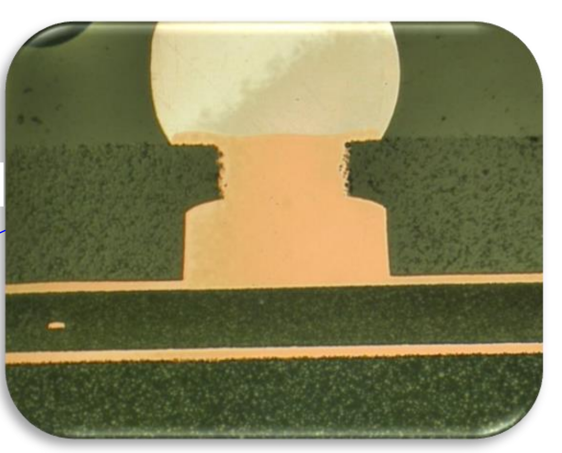
FOLP® Elemental Technology （2）

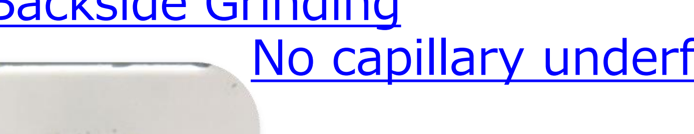
Applied Model
AiP Case

Detail of Via bottom

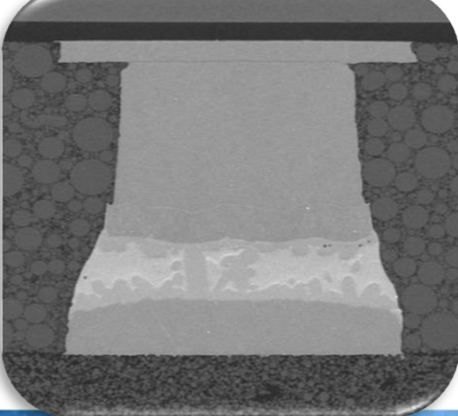
New Through Via Type②
ToM(Terminal on Mold)







C4 bonding



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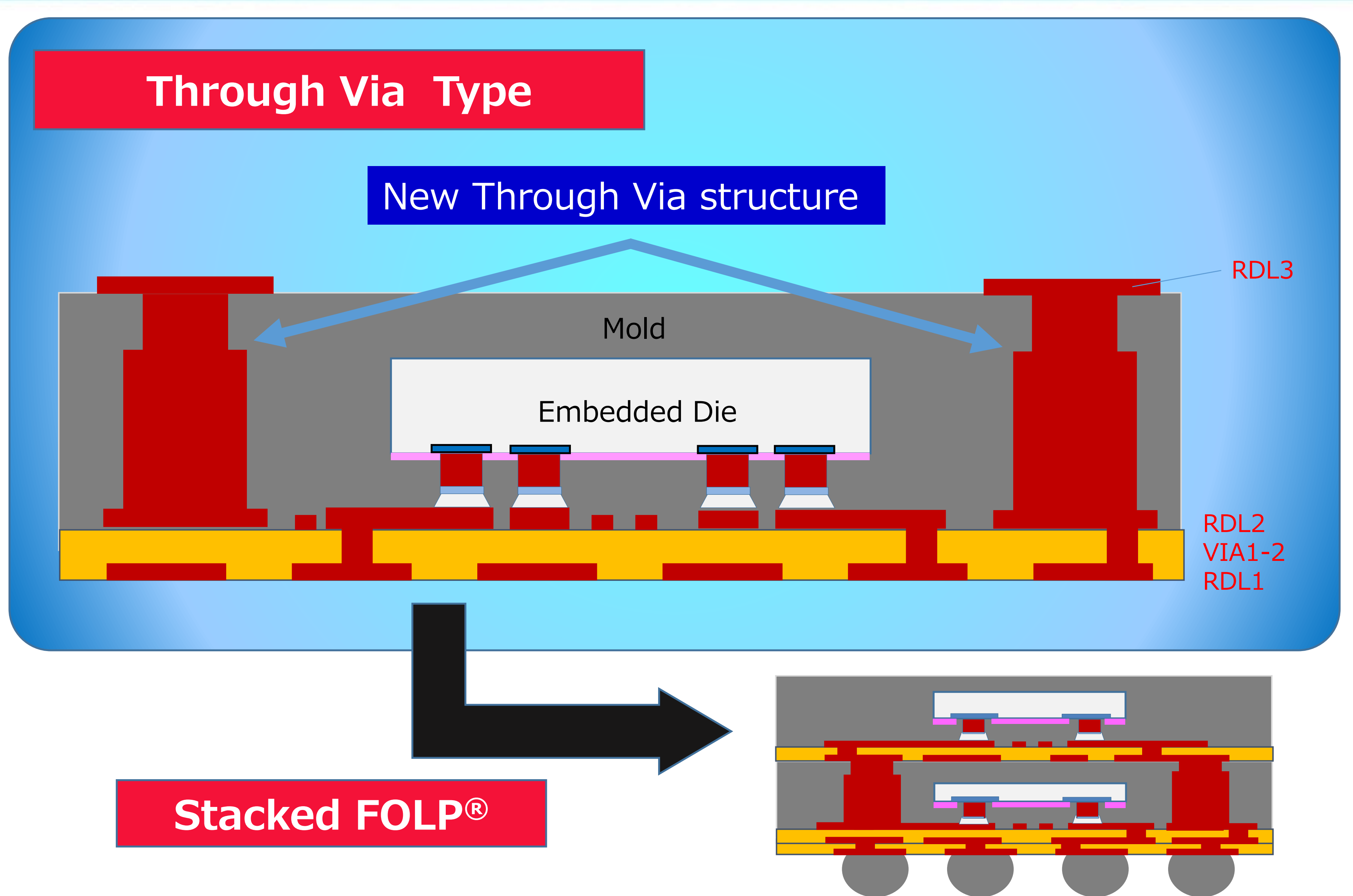
Stacked FOLP®



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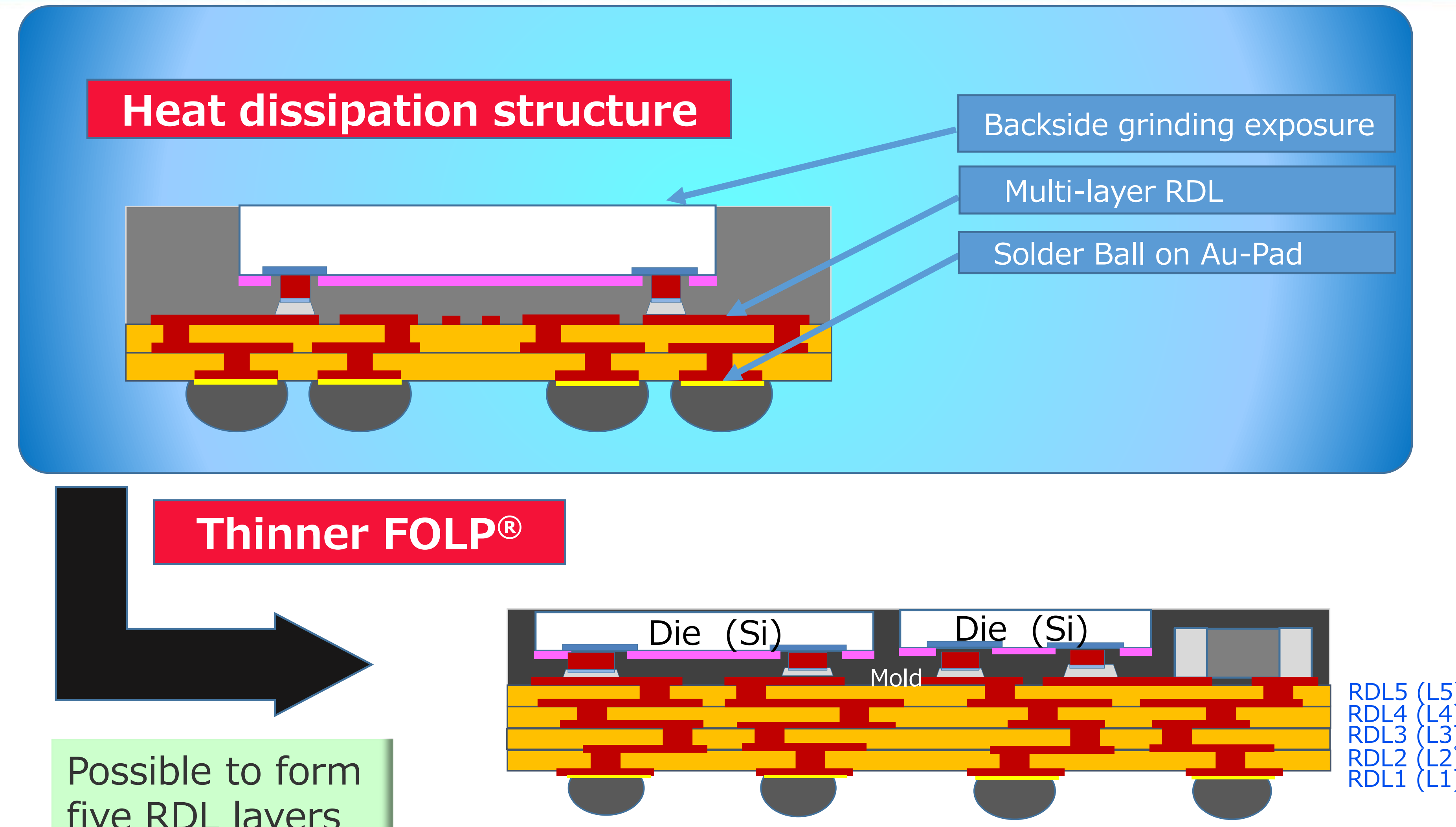
Active＋Passive Device FOLP® Module



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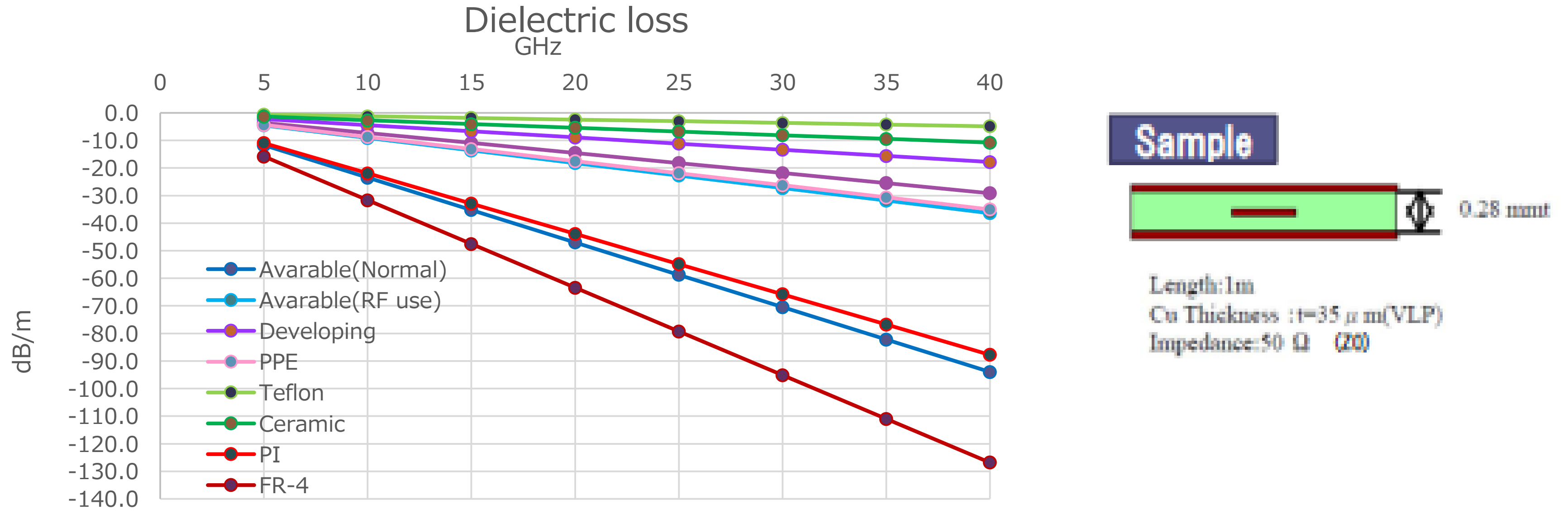
FOLP® Isolation Materials for RF devices



Type	Film thickness	Dk			Df			Breakdown Strength (kV/mm)
		20GHz	40GHz	60GHz	20GHz	40GHz	60GHz	
Normal	35umt（Typical)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Thick film	～200umt	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Low stress	35umt（Typical)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
RF	35umt（Typical)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Developing	35umt（Typical)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	

Please feel free to contact us about the isolation material characteristics.

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Technology Roadmap

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FOLP® Technology Roadmap

Multi-Layer, 3 D FOLP®

Stacked Type

Thinner , Heat dissipation FOLP®

AiP Type

Antenna

Antenna

Multi-Layer Type

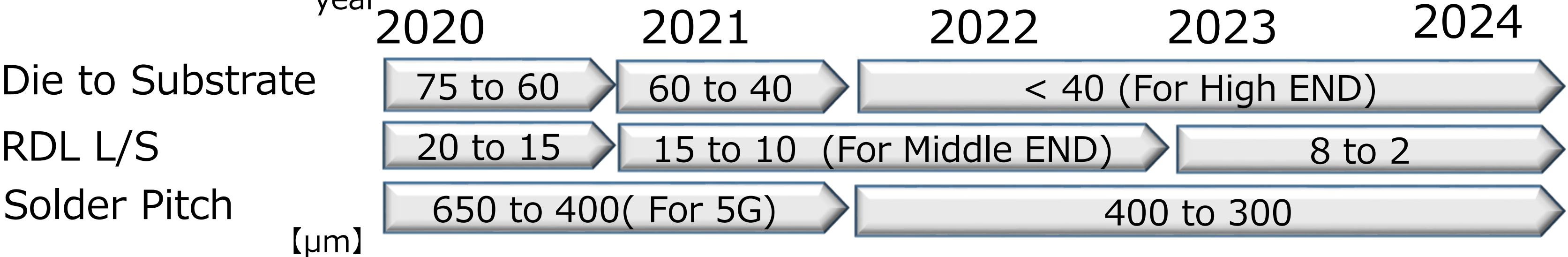
5G

Small, Fine pitch FOLP®

Normal Type

Wearable＆Robotics

APE+Memory



year	2020	2021	2022	2023	2024
Die to Substrate	75 to 60	60 to 40	< 40 (For High END)		
RDL L/S	20 to 15	15 to 10 (For Middle END)		8 to 2	
Solder Pitch	650 to 400(For 5G)		400 to 300		

【μm】

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Reliability

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Reliability results

FOLP® SPEC.

【FOLP®】	【Si Chip】
Size :4.1mmSQ	Chip Size :2.1×3.0mm
Terminal Pitch :0.4mm	Cu Pillar :Pitch :75μm
Height :0.7mm	Diameter :40μmΦ
I/O count :64pin	

Items	Condition	N count	Result
MSL Level 1	85℃/85% 168hr ⇒260℃ 30sec 3 times	22	No fail
PCT (PKG)	Pre-condition ⇒121℃ 100% 500cyc	22	No fail
HTHH (PKG)	Pre-condition ⇒85℃ 85%RH 1000hr	22	No fail
HTS (PKG)	Pre-condition ⇒150℃ 168hr , 500hr , 1000hr	22	No fail
TCT (PKG)	Pre-condition(each 15min/RT2min) ⇒-65℃～RT～150℃ 1000cyc	22	No fail
Drop Test (Board)	JEDEC【JESD22-B111】 1500G time : 0.5msec	2	MTTF 546 times 1ST Fail 76 times Pass/Fail :30 times

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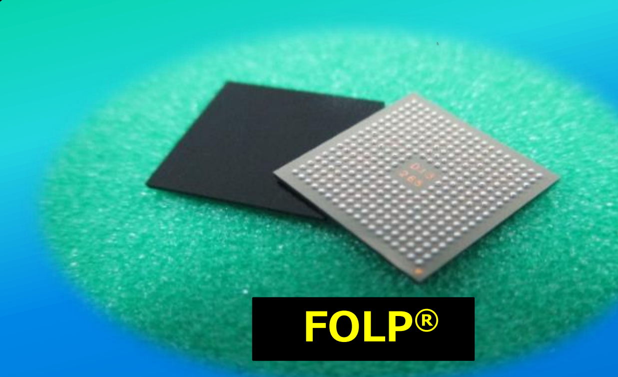
AOI-ELECTRONICS's FOLP® supports IoT Technologies



IoT/M2M Communication module
LTE / 5G / WiMAX / Z-Wave / ZigBee / Bluetooth / RFID
NFC/ Transfer Jet / Felica / PLC / Tuner / GPS /

Sensor / MEMS Device
CIS / Compass / Tunable capacitor

Analog / Power / Driver / RF / Memory ICs
PMIC / RF / BaseBand / Swich / Converter / Battery
Control /Flash / DRAM/ OLED control SoC / Others

Automotive ICs
Radar system/ RF tuner for Navigation systems

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