

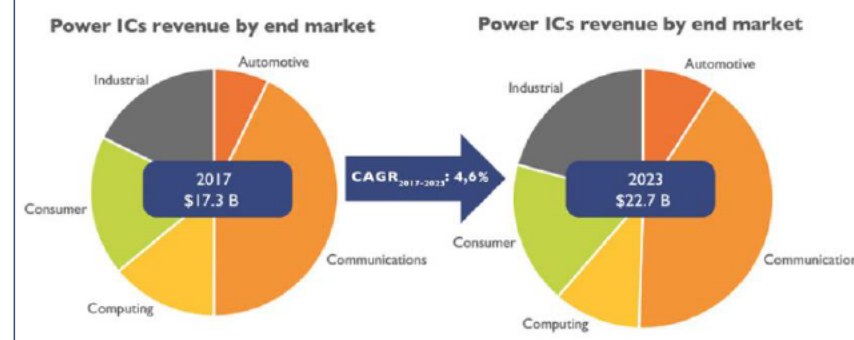
# Flip Chip QFN with Cu-pillar

# Flip Chip QFN with Cu-pillar

## Power ICs market revenues (in \$B)

(Source: Introduction to the Power IC market 2018, Yole Développement, October 2018)

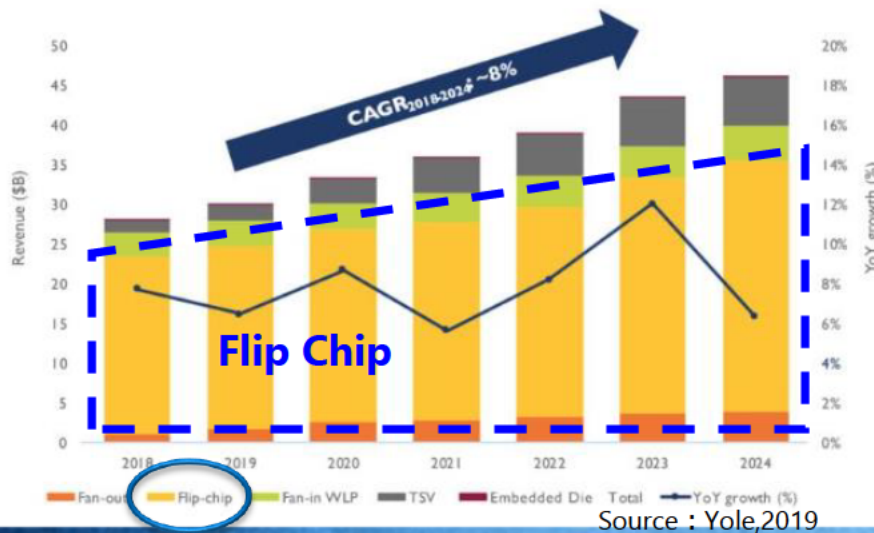
Large market share of LDO and DC-DC converter ICs



(Source: Yole Développement)

## 2018-2024 advanced packaging revenue forecast split by platform

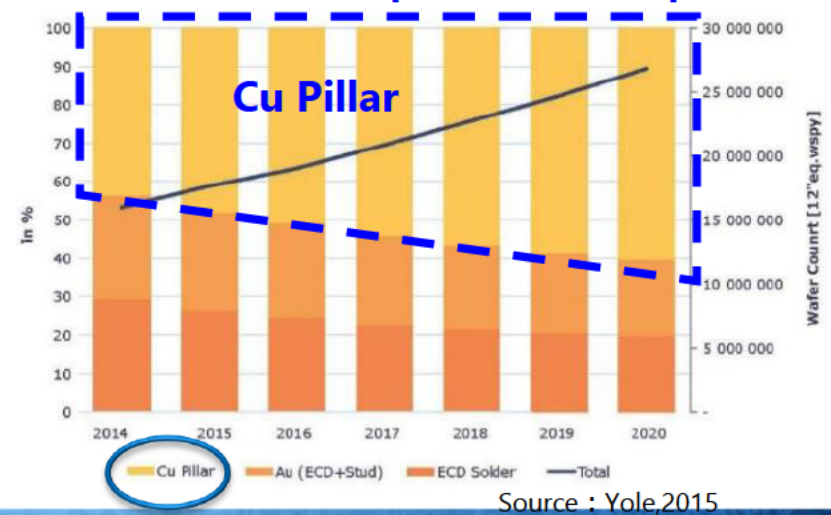
(Source: Status of the Advanced Packaging Industry 2019 report, Yole Développement, 2019)



Source : Yole,2019

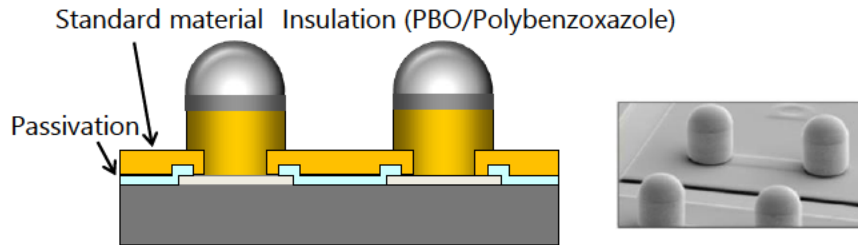
## Flip Chip Capacity forecast breakdown by Flip Chip Technology

### Cu-pillar Market expansion



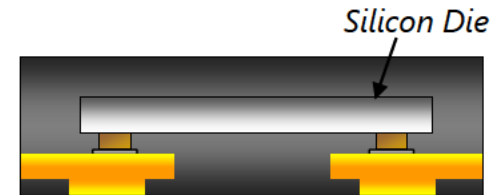
Source : Yole,2015

## ◆ OUME Electronics : Cu Pillar Bump Over 10 years of experience



- Form solder height up to 1/2 of pillar dia.
- Formable up to 20um Pillar dia.
- RDL lamination layer  
(Sample result; 3 layers)  
...Under development

## ◆ AOI Electronics : Package Assembly



- Flip-chip C4.
- Large format matrix Lead frame
- Wettable flank  
...Under development

*Turnkey processing*



① **Sub 6GHz(RF) : RF-Switch/Antenna Tuning Switch etc.**  
⇒ **Low Coff, Low Insertion loss**

② **Power IC : DCDC Converter IC, LDO, PMIC etc.**  
⇒ **Low Inductance(Low EMI), Low Resistance**

**for Automotive Fsw;2MHz↑、Wettable flank**

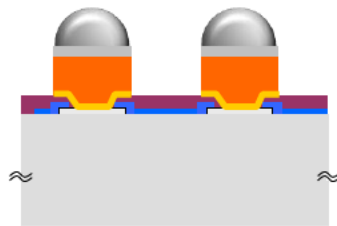
# Flip Chip QFN with Cu-pillar

## Cu Pillar/Micro Bump technology road map

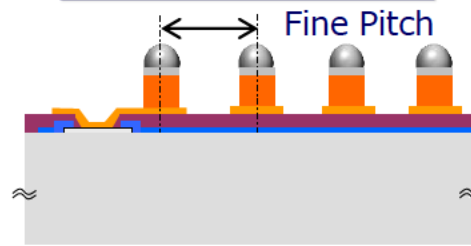
We can offer Cu Pillar Bump/Micro Bump as a terminal for flip chip connection. [Unit :  $\mu\text{m}$ ]

Road Map		Typical			2021/M~			2022		
SIZE		6inch	8inch	12inch	6inch	8inch	12inch	6inch	8inch	12inch
Standard	Bump Space	NA	75	75	75	60	60	70	60	60
	Min terminal diameter	NA	75	75	75	60	60	70	60	60
	Max terminal height	NA	65	65	53	70	70	65	70	70
Custom	Bump Space	NA	50	70	NA	40	40	NA	35	35
	Min terminal diameter	NA	50	70	NA	40	40	NA	35	35
	Max terminal height	NA	50	45	NA	65	45	NA	70	50
Terminal structure		SnAg/Cu			SnAg/Ni/Cu (8inch) SnAg/Cu			SnAg/Ni/Cu SnAg/Cu		

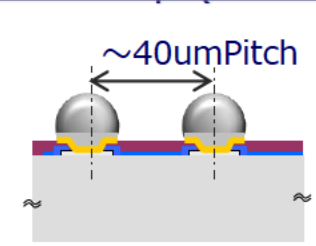
Cu Pillar Bump



Cu Pillar with RDL



Micro Bump (Solder)





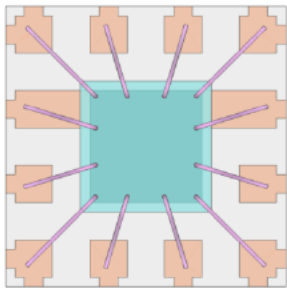
# Flip Chip QFN with Cu-pillar

## Advantage : Miniaturization and High functionality

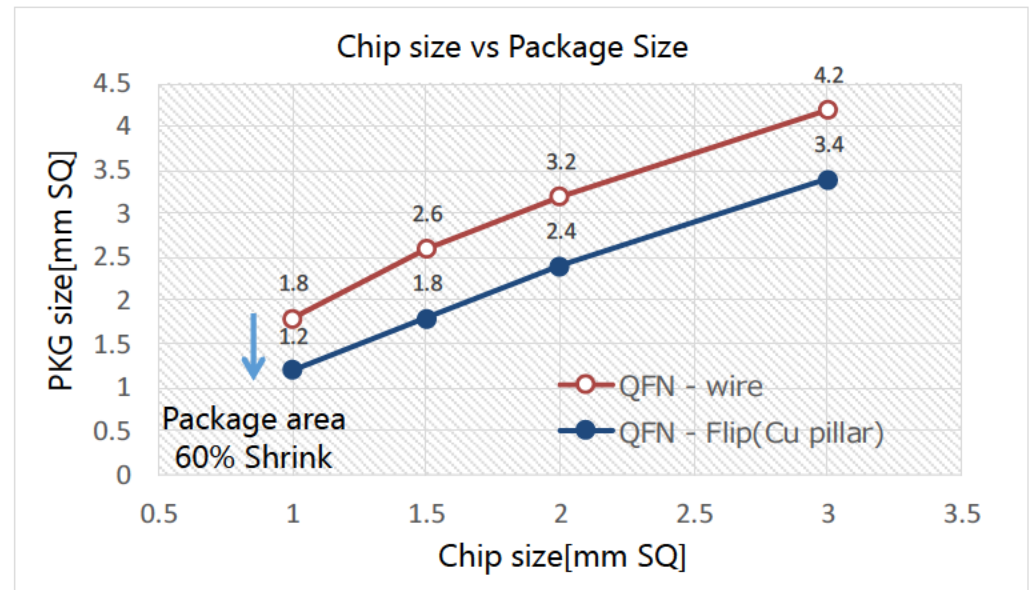
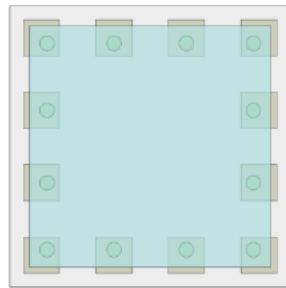
No.	①	②	③
Package size	1.5mm SQ	1.5mm SQ	2.2mm SQ
Chip size	1.33mm SQ	0.7mm SQ	1.33mm SQ
PKG structure	QFN Flip chip	QFN wire	

### Package structure

#### Wire type



#### Flip chip type



Expected to be Miniaturization and highly functional (large chip size can be installed)

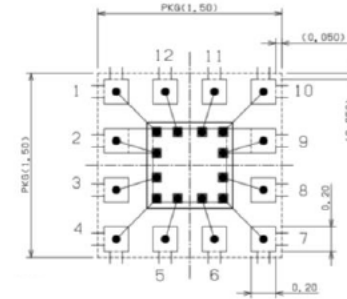
# Flip Chip QFN with Cu-pillar

## Advantage : Low Electrical Parasitic properties

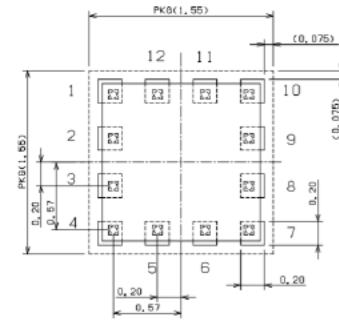
Electrical Parasitics Comparison (Per one)

	QFN - wire	FC-QFN(Cu pillar)
Package size [mm]	1.5mmSQ	1.5mmSQ
Chip size [mm]	0.70x0.70	1.33x1.33
Lead frame thickness	Cu 0.125mmt	Cu 0.125mmt
Internal wiring	Au wire $\Phi$ 23 $\mu$ m	Cu pillar $\Phi$ 80 $\mu$ m/Height50 $\mu$ m
Terminal size	0.2x0.2mm	0.2x0.2mm
L : Inductance [nH]	0.79	0.02
R : Resistance [m $\Omega$ ]	47.70	0.22

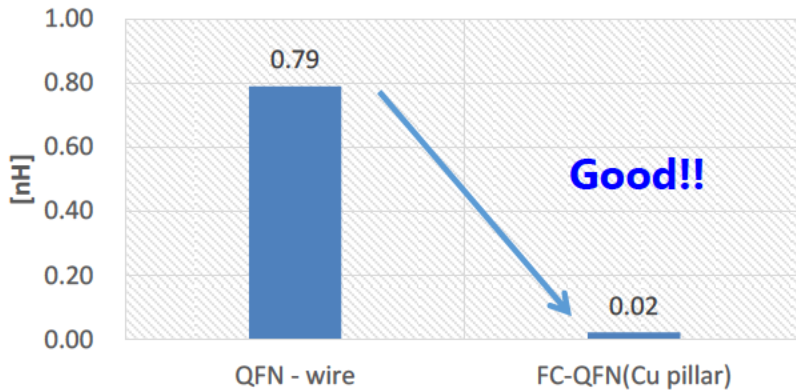
QFN-Wire



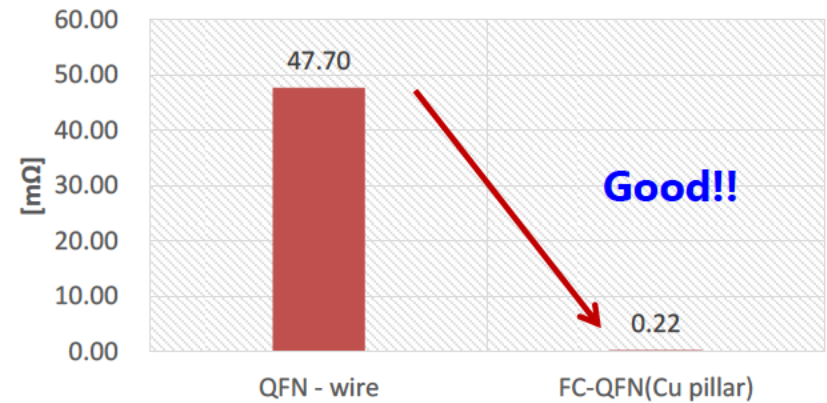
FC-QFN (Cu-pillar)



**L : Inductance**



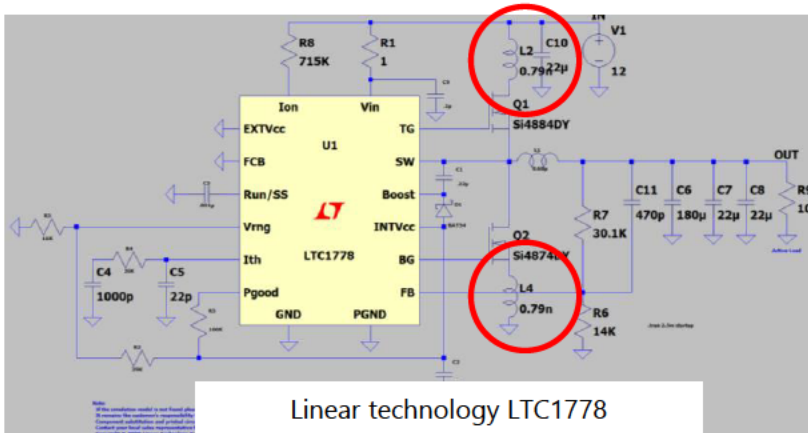
**R : Resistance**



Flip chip QFN Package can achieve **Low Inductance** and Low Resistance. Expected to improve ripple in DC-DC converter IC.

# Flip Chip QFN with Cu-pillar

## LTSpice @ Step down DC-DC Converter IC



Added parasitic Inductance

QFN wire :  $L=0.79\text{nH}$   
 FC-QFN(Cu-pillar) :  $L=0.02\text{nH}$   
 @frequency:500kHz

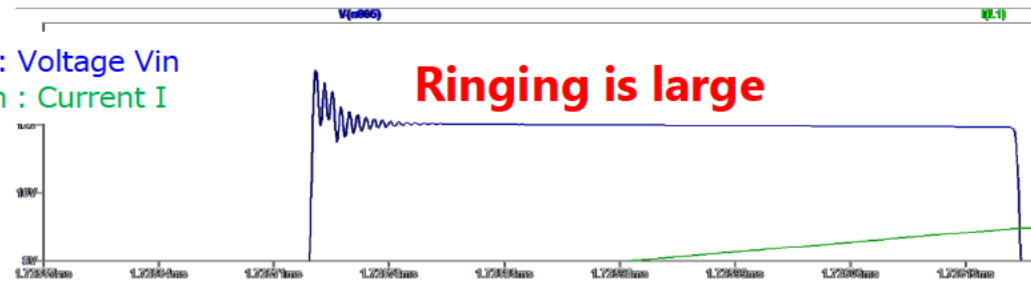
Ringing in 250MHz class

SW node(Drain-Source) oscillation

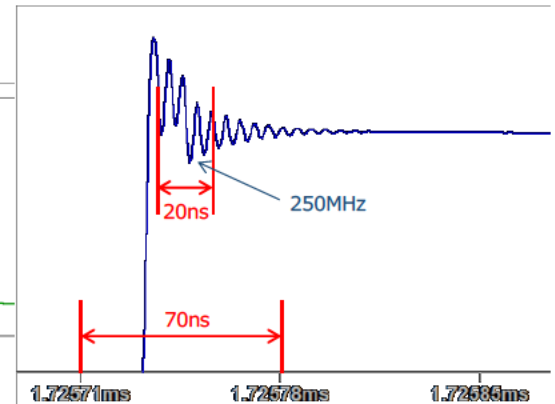
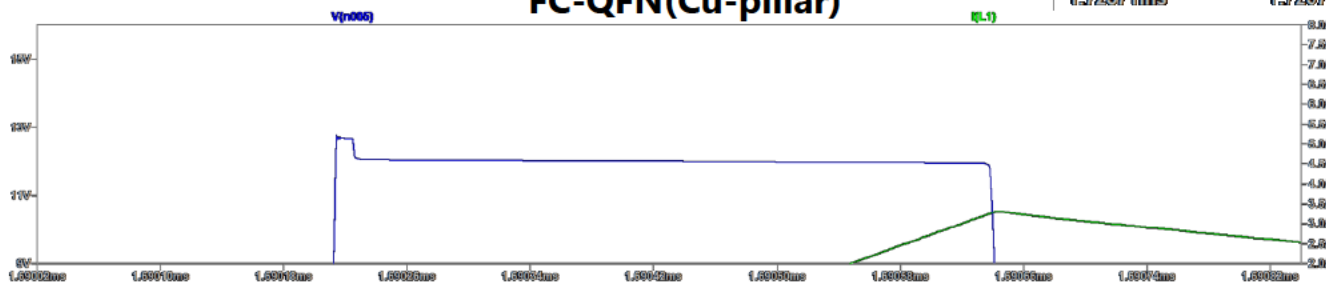
QFN wire

Blue : Voltage  $V_{in}$   
 green : Current  $I$

**Ringing is large**



FC-QFN(Cu-pillar)



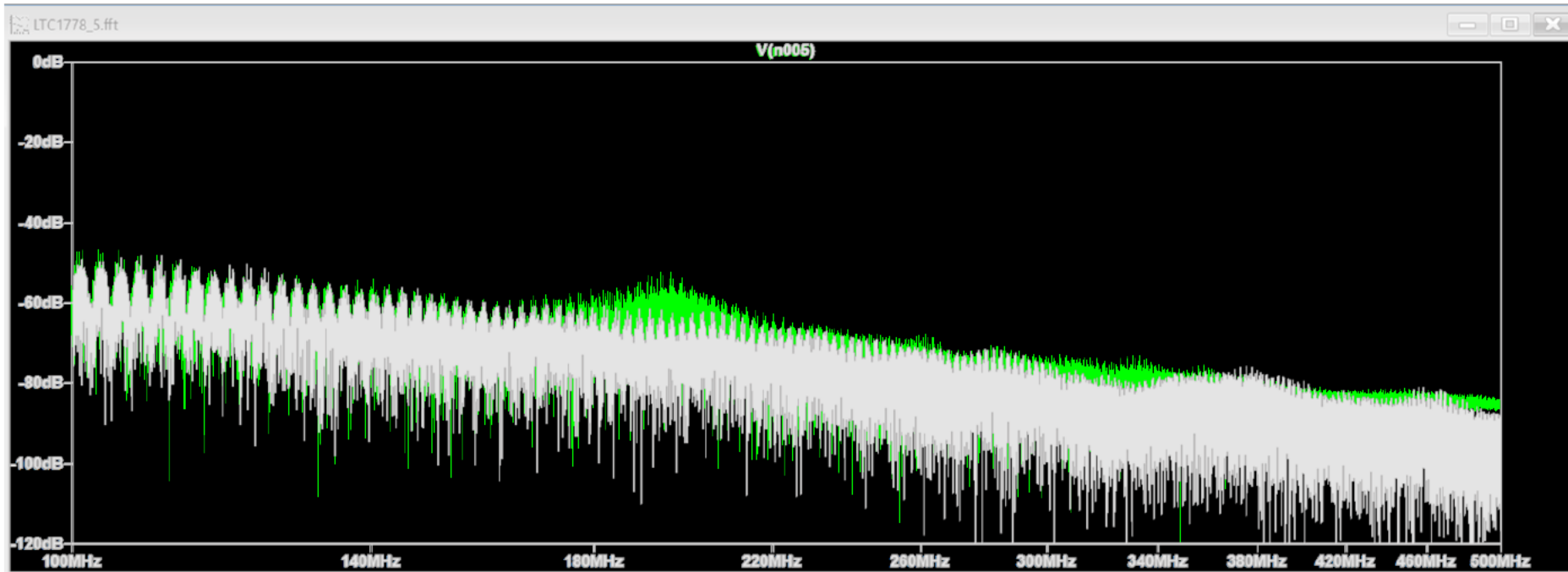
# Flip Chip QFN with Cu-pillar

## LTSpice @ Step down DC-DC Converter IC

FFT Output frequency analysis

QFN wire 0.79nH(green)

FC-QFN 0.02nH(gray)

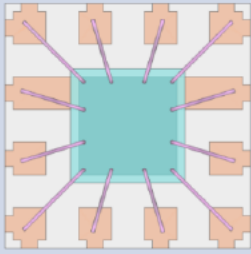
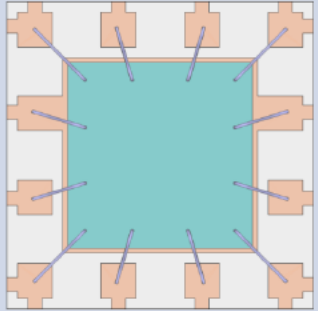
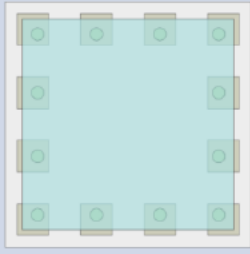


EMI improvement is about 10 dB@200MHz.  
EMI improvement of 3 to 5 dB above 220MHz.



# Flip Chip QFN with Cu-pillar

## Thermal resistance Simulation(steady state)

		QFN wire A	QFN wire B	QFN Flip chip
Package structure				
Package size		1.5mm SQ	2.2mm SQ	1.5mm SQ
Chip size		0.7mm SQ	1.33mm SQ	1.33mm SQ
4-layer board (No via)	Thermal resistance [°C/W]	153	103	88.4
	PD [W]	0.65	0.97	1.13

- Boundary condition
  - Atmospheric temperature : 0°C ※Assumption: No radiant heat dissipation
  - Calorific value : 1W ( The heat generation density is set uniformly on the chip surface. )
  - Heat transfer coefficient : 10 W/(m<sup>2</sup>C) ※Natural air cooling
- Mounting board
  - 1/2 symmetry (JEDEC51-7, 4-layer board 38.1x114.3x1.6)

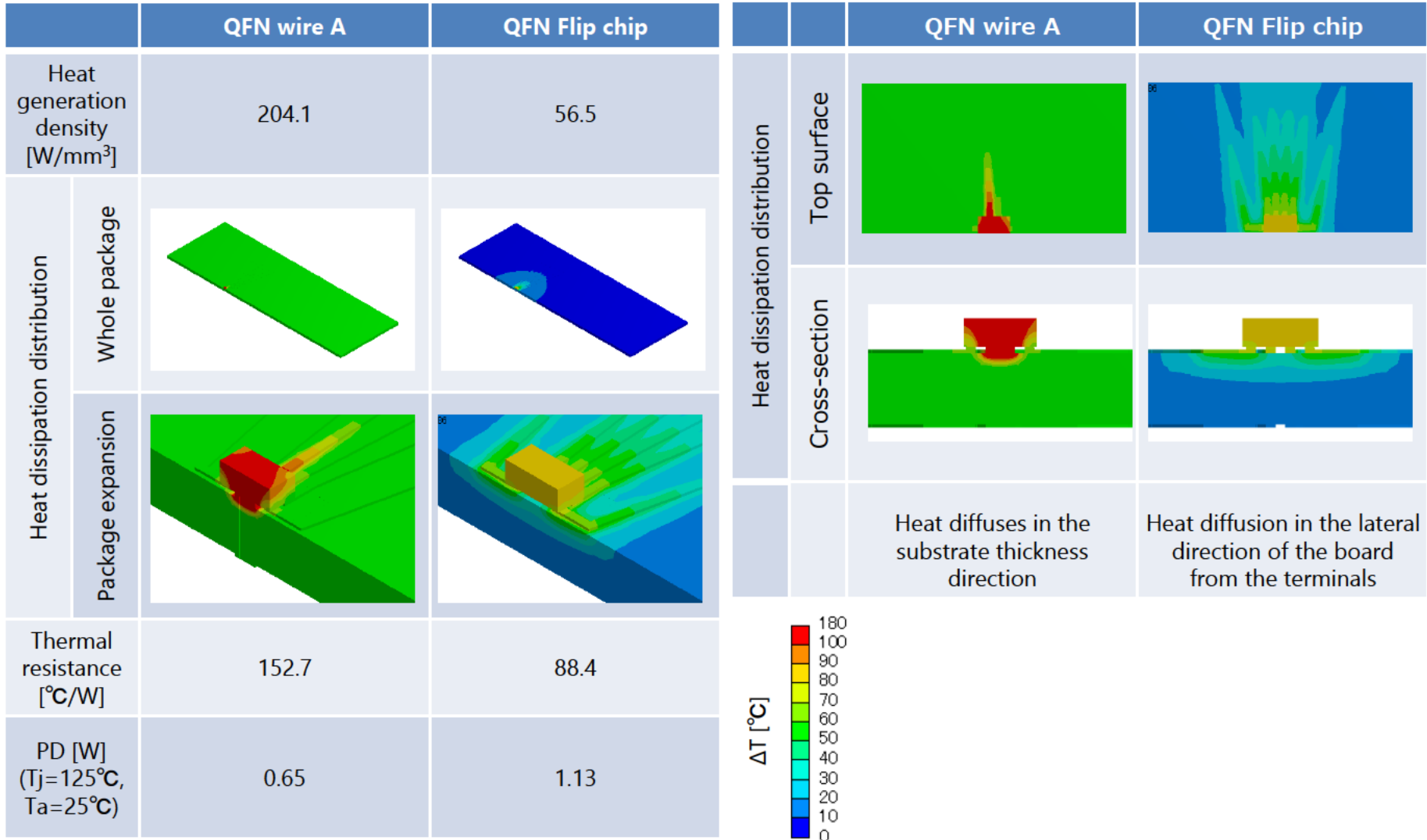
※ PD : T<sub>j</sub>=125°C, T<sub>a</sub>=25°C

The heat generation density is small due to the large chip area of FCQFN



# Flip Chip QFN with Cu-pillar

## Thermal resistance Simulation(steady state)



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